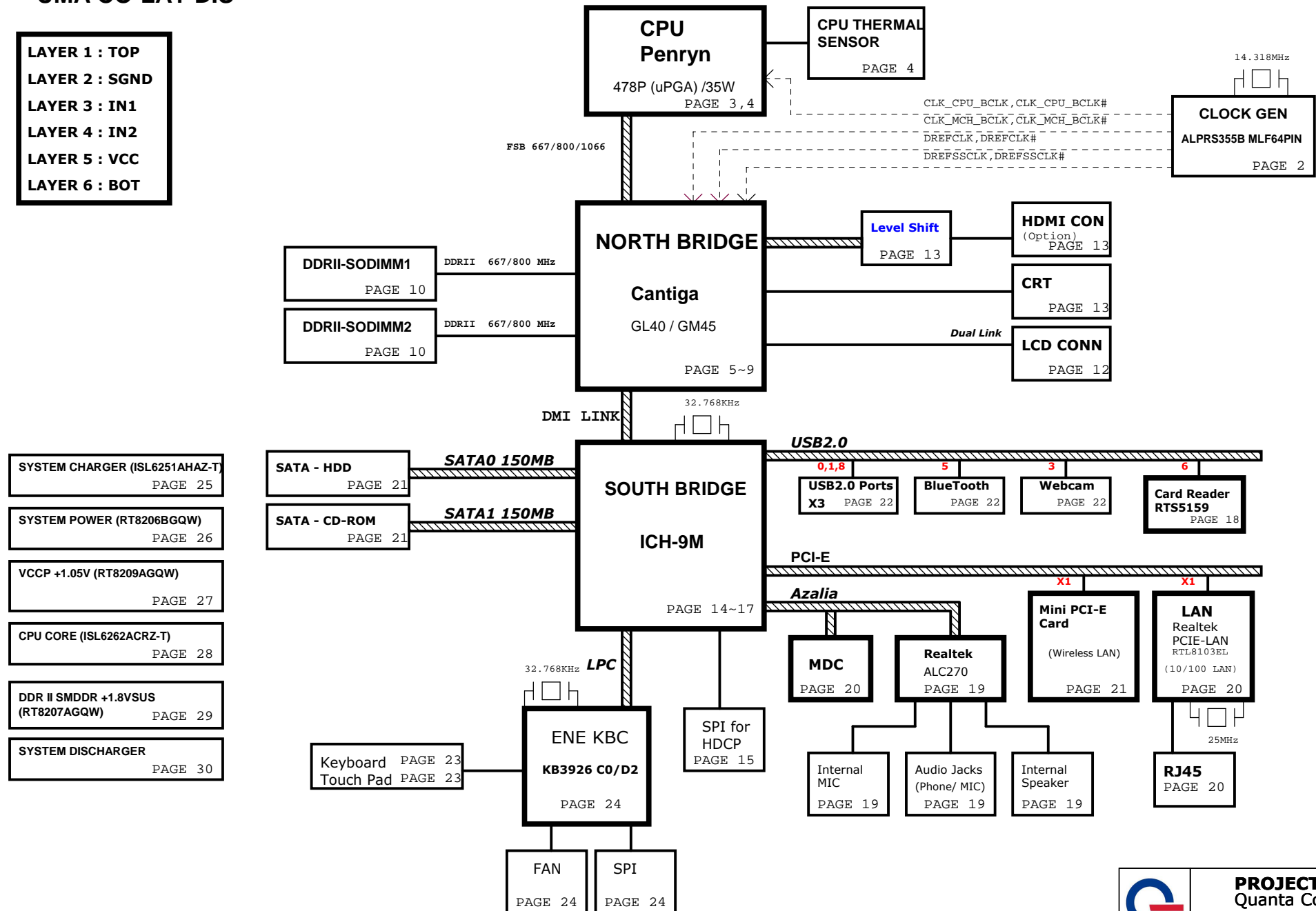


PCB STACK UP
6L UMA CO-LAY DIS

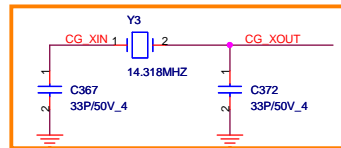
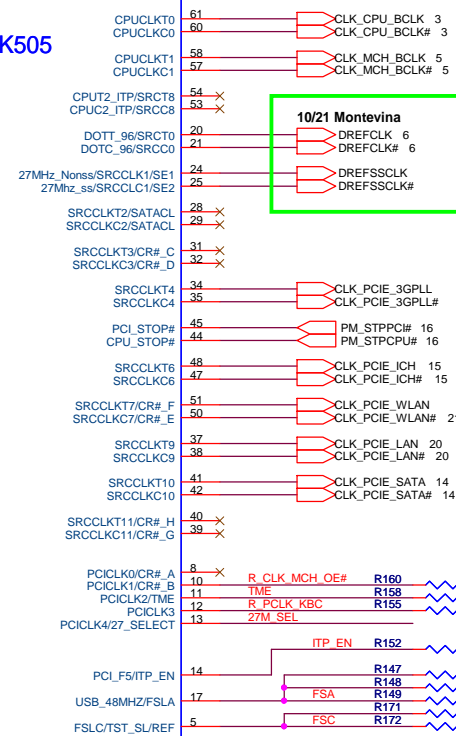
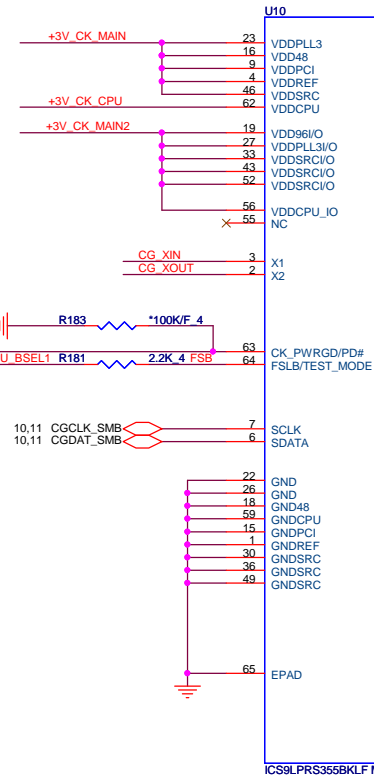
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

Wimbledon AX3/5 BLOCK DIAGRAM



PROJECT :AX3
Quanta Computer Inc.

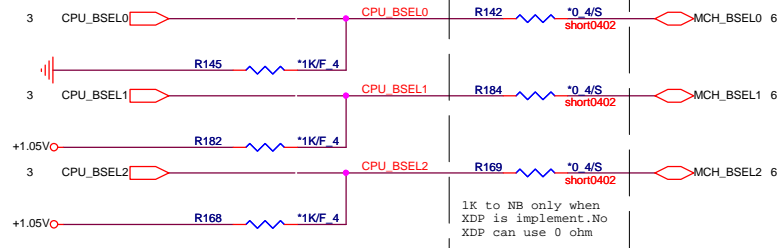
Size Custom	Document Number	Rev 2A
Block Diagram		
Date: Friday, January 29, 2010	Sheet 1 of 30	



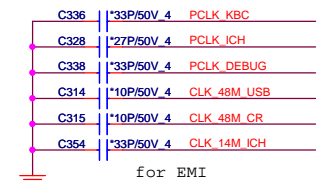
0=UMA
1 = External VGA

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

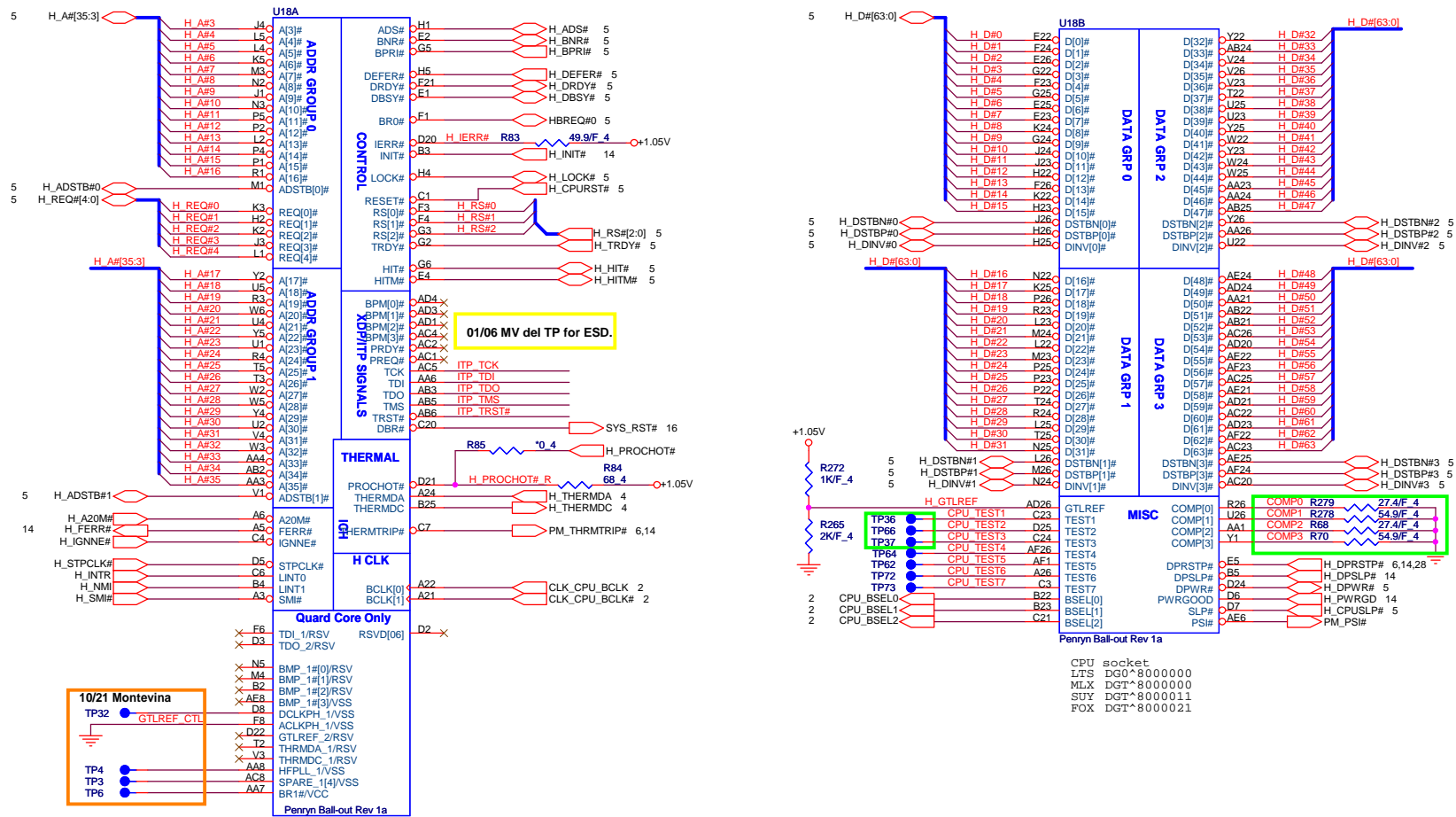
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
ICS	ICS9LPRS355BKLFT	ALPRS355000



FSC	FSB	FSA	CPU	SRC	PC
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



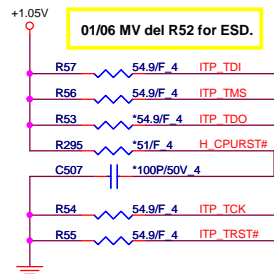
Size Custom	Document Number Clock Generator	Rev 2A
Date: Tuesday, February 23, 2010		Sheet 2 of 30



	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quad Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

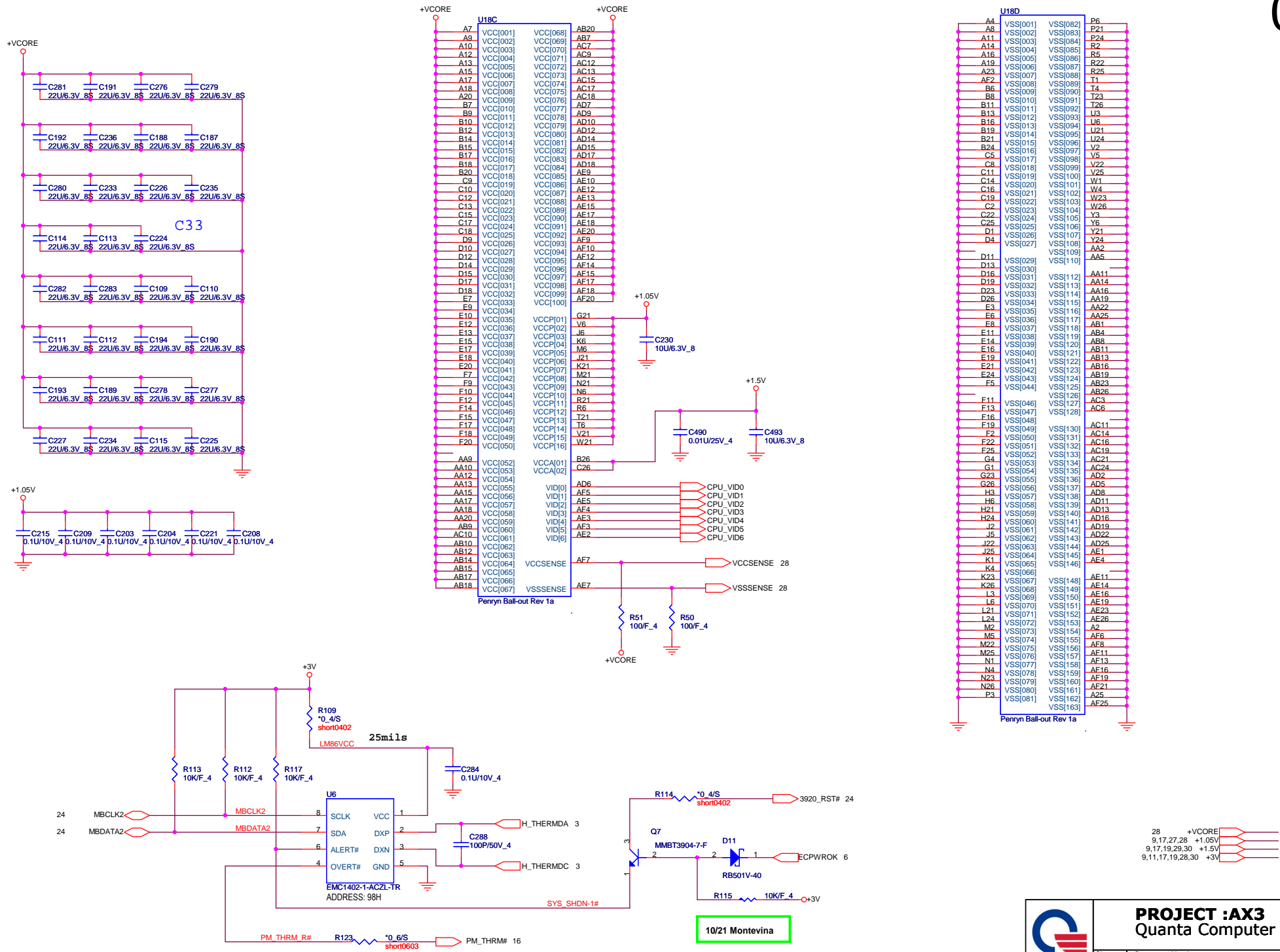
10/21 Montevina

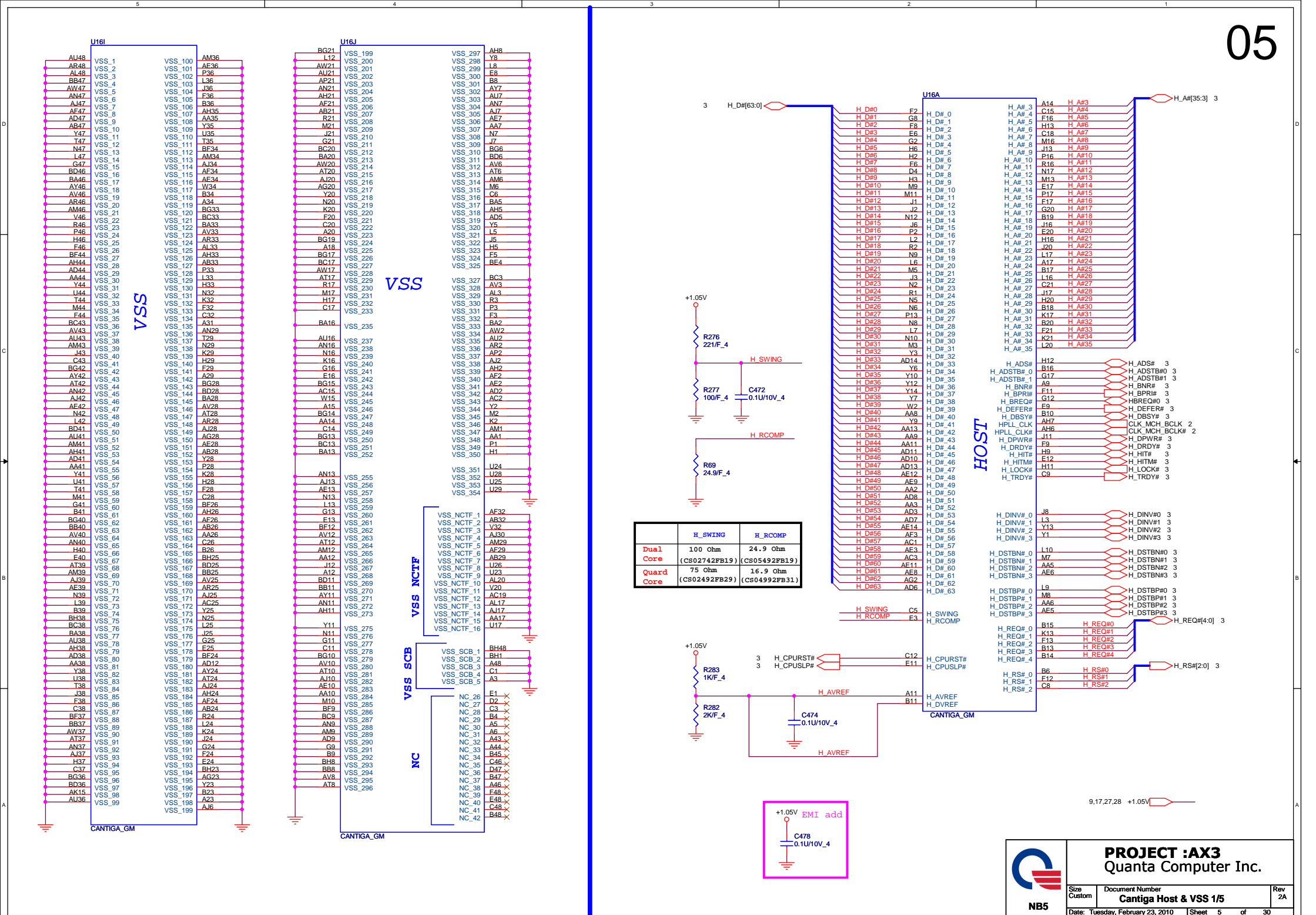
Populate ITP700Flex for bringup

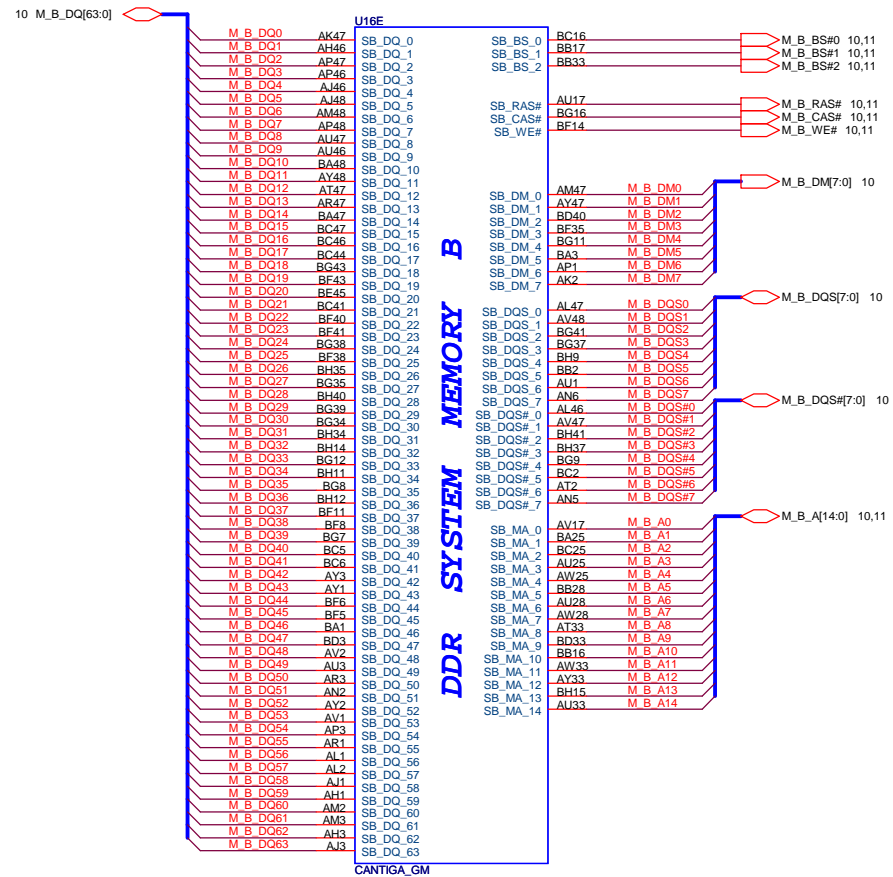
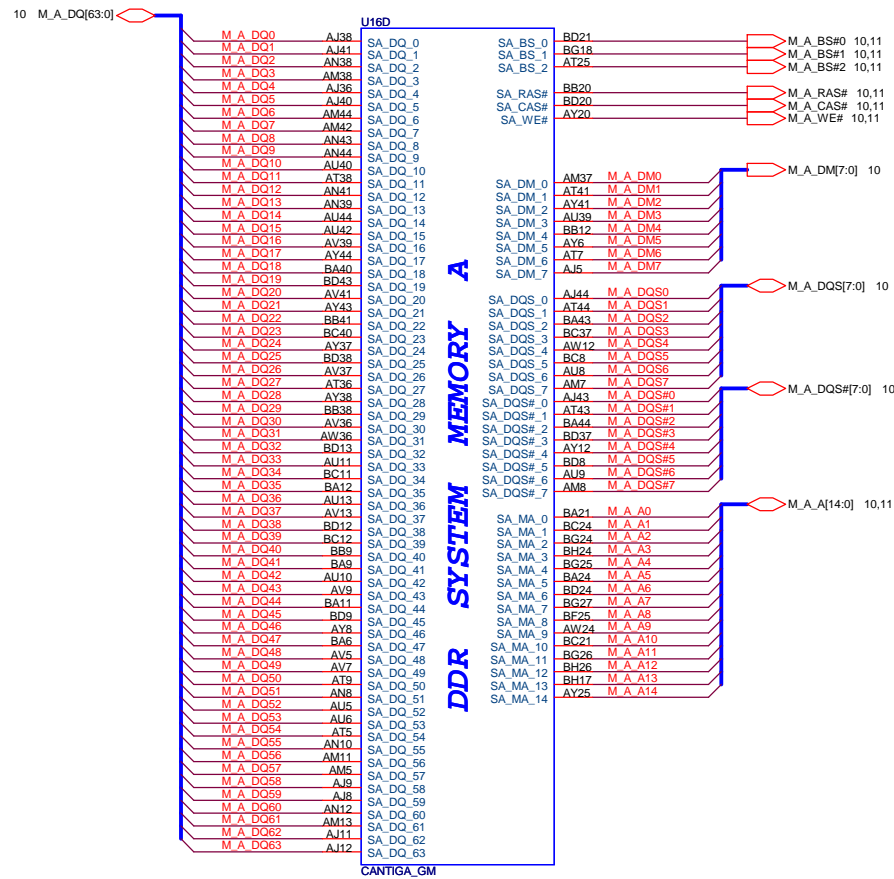


9,17,27,28 +1.05V


PROJECT :AX3
 Quanta Computer Inc.

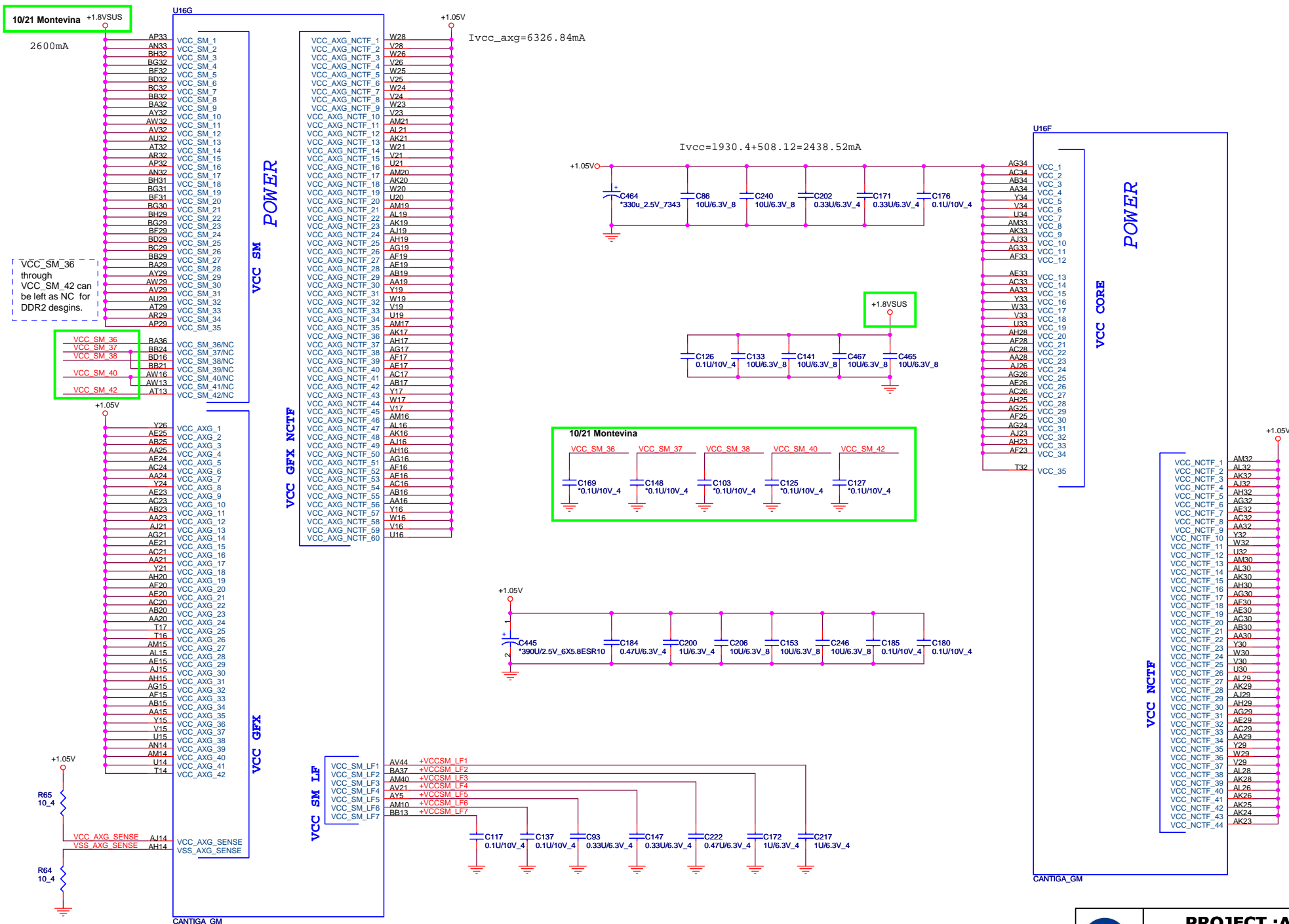




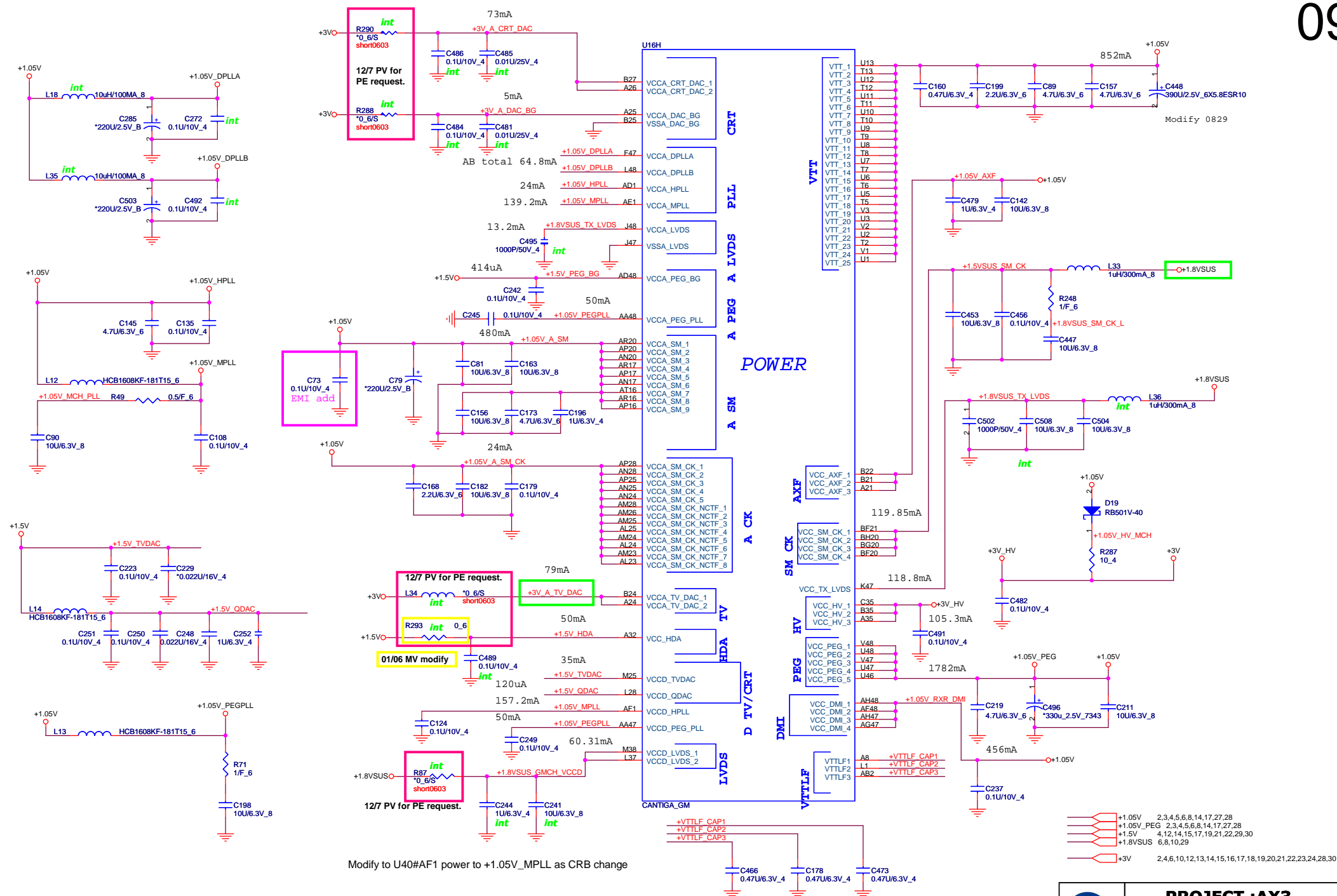


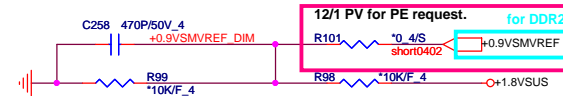
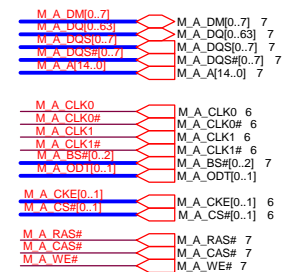
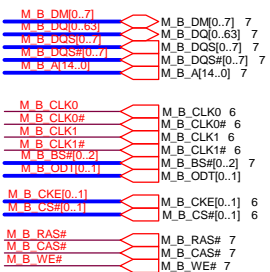
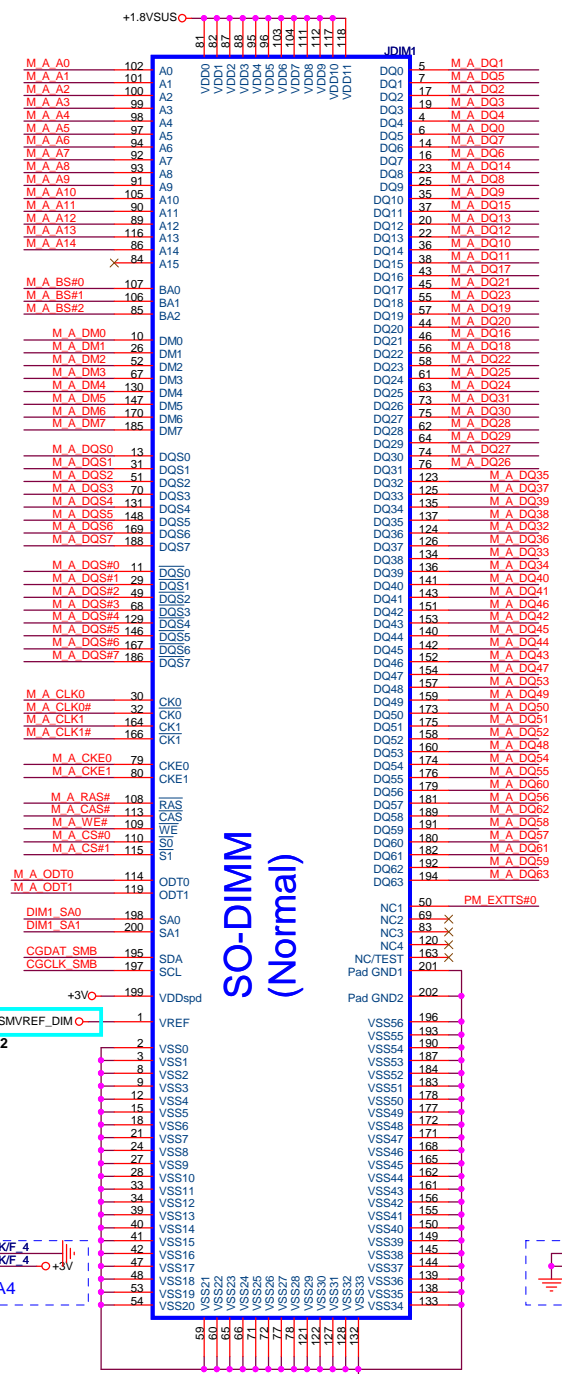
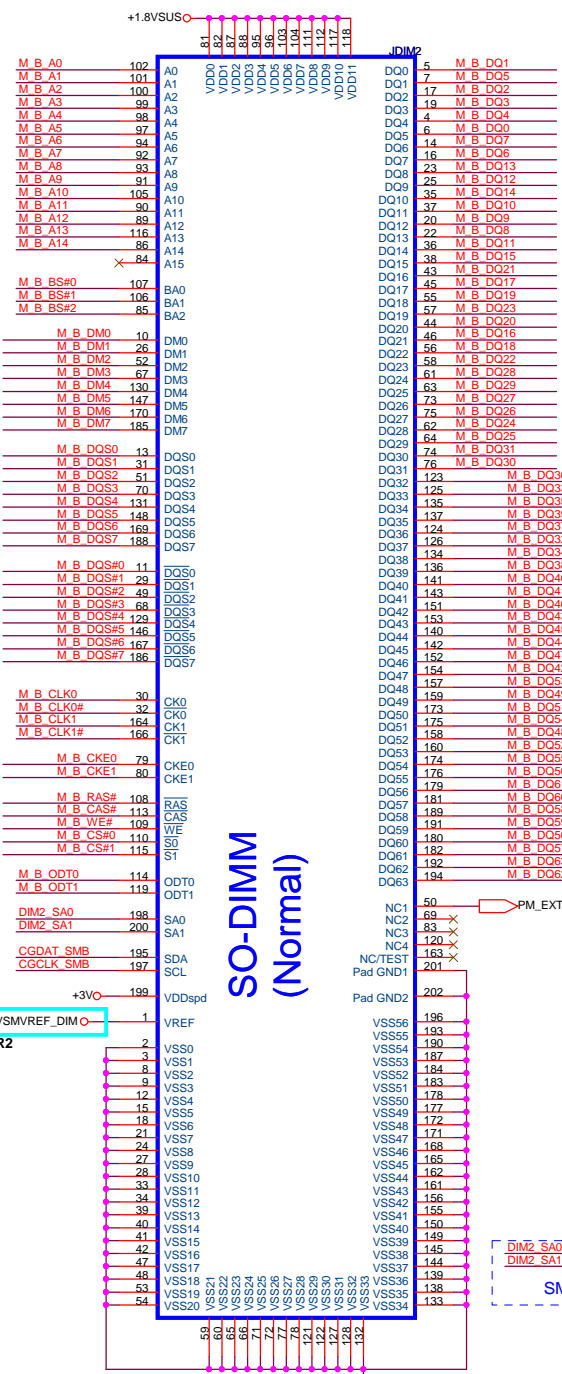
PROJECT :AX3
Quantia Computer Inc.

Size Custom	Document Number Cantiga DDR3 3/5	Rev 2A
Date: Tuesday, February 23, 2010	Sheet 7 of 30	

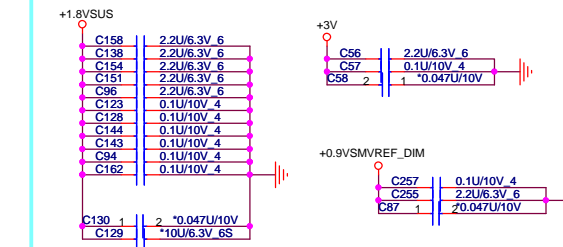


9,17,27,28 +1.05V
9.29 +1.8VSUS

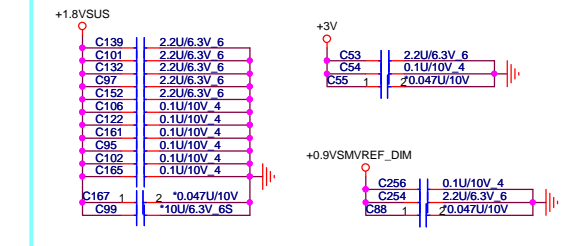




Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

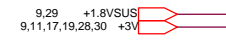


Place these Caps near So-Dimm2.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

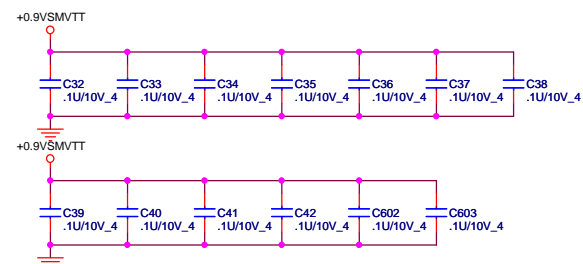


PROJECT :AX3
Quanta Computer Inc.

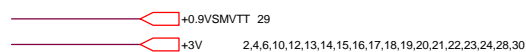
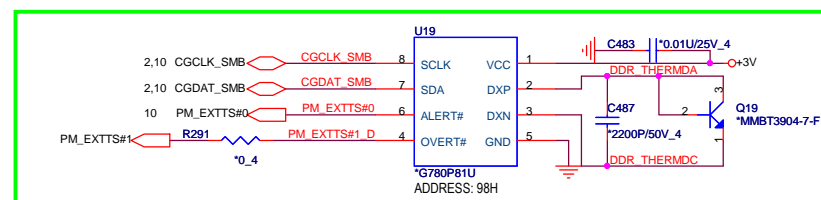
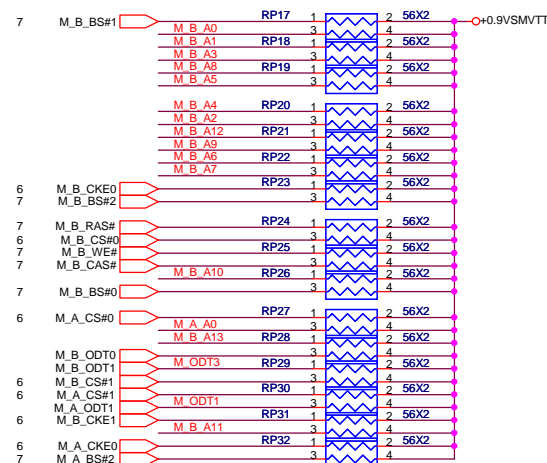
Size Custom	Document Number	Rev 2A
	DDR2 DIMM	
Date: Tuesday, February 23, 2010	Sheet 10 of 30	



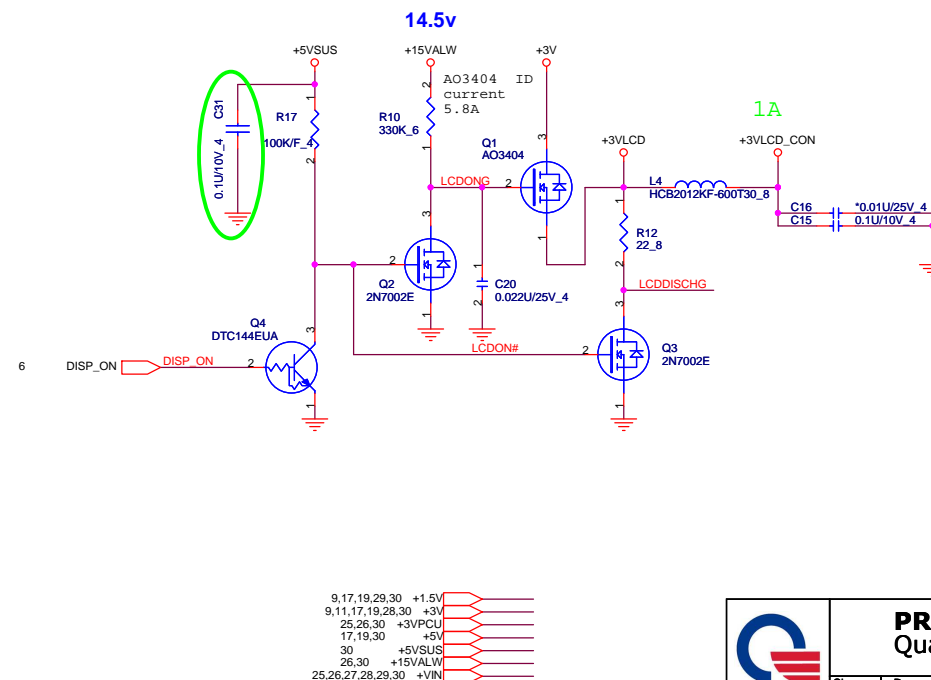
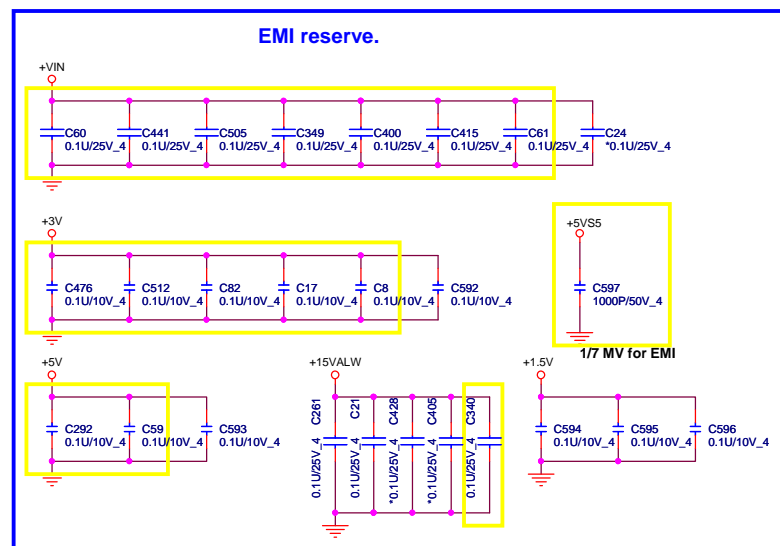
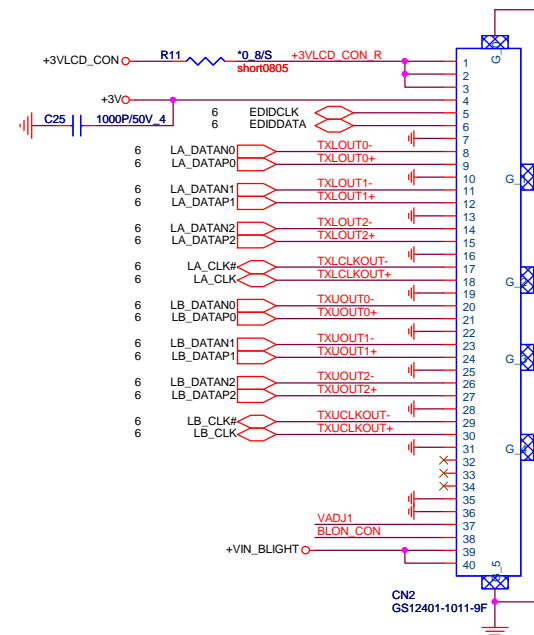
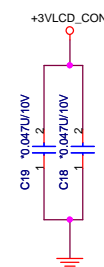
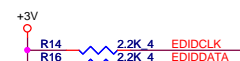
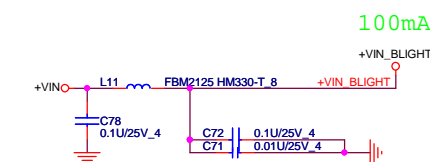
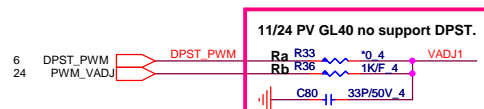
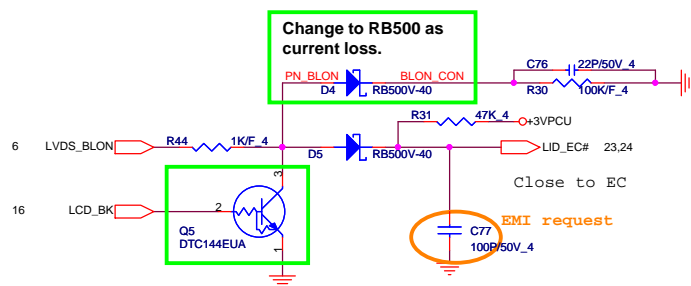
DDR II B CHANNEL



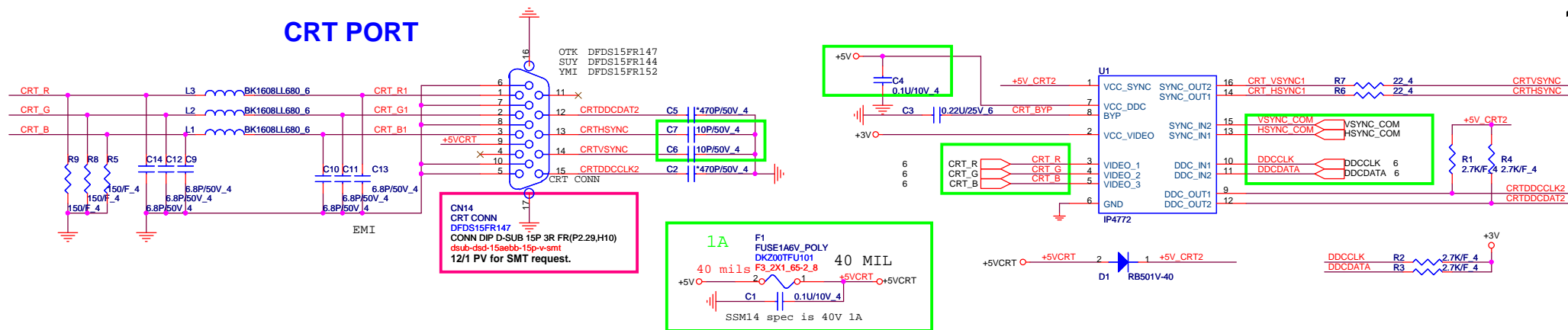
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



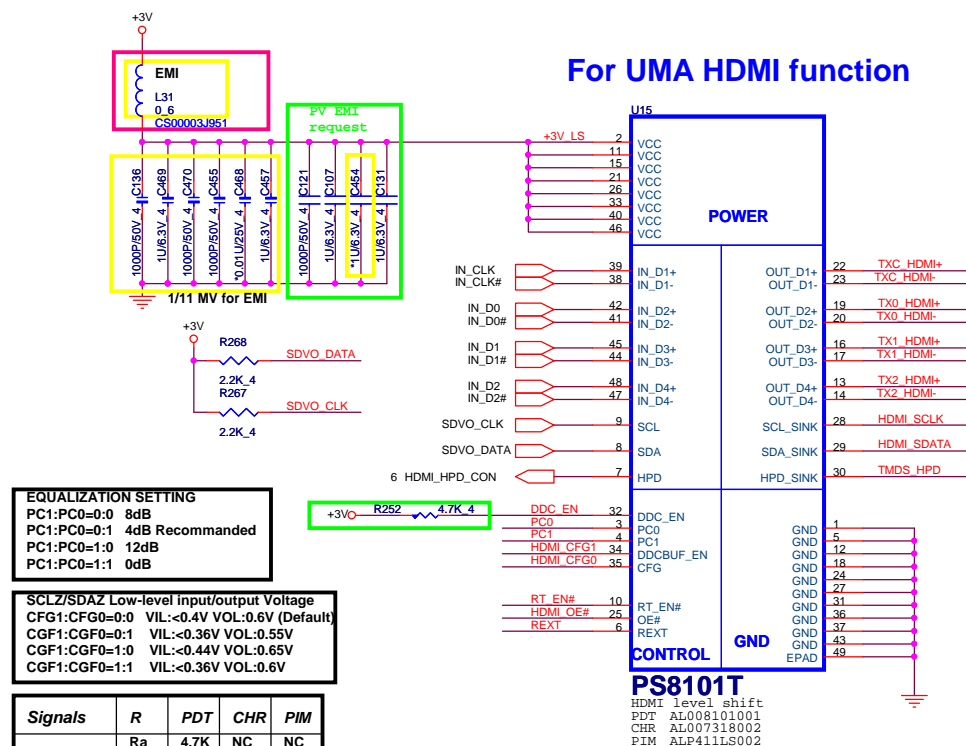
LID Switch



CRT PORT



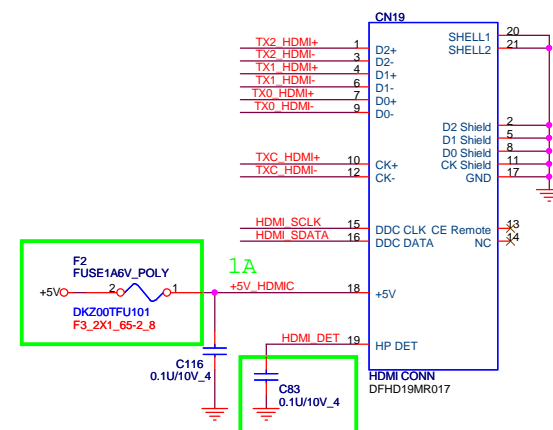
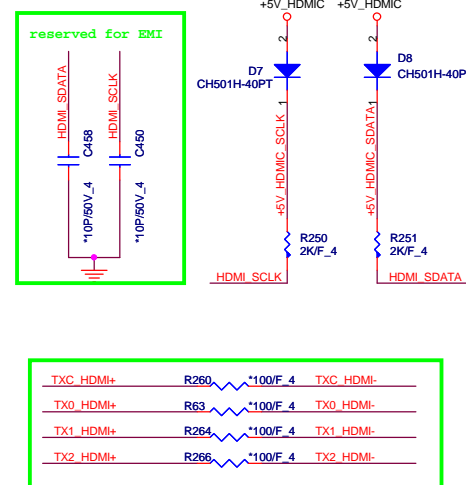
For UMA HDMI function



9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella
CHR : need Na R1182, add R1027 for capella

Vendor:PDT P/N:AL008101001

Vendor:PTM P/N:ALP4111.S002

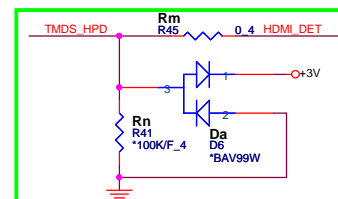


EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage	
CFG1:CFG0=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1	VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0	VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1	VIL:<0.36V VOL:0.6V

<i>Signals</i>	<i>R</i>	<i>PDT</i>	<i>CHR</i>	<i>PIM</i>
PC0	Ra	4.7K	NC	NC
	Rb	NC	NC	0
PC1	Rc	NC	10K	NC
	Rd	NC	NC	0
HDMI_CFG0	Re	NC	10K	NC
	Rf	NC	NC	0
HDMI_CFG1	Rg	NC	10K	NC
	Rh	NC	NC	0
REXT	Ri	499	1.2K	0
RT_EN#	Rj	NC	NC	0
HDMI_OE#	Rk	NC	0	0

<i>Detect</i>	<i>R</i>	<i>PDT</i>	<i>CHR</i>	<i>PIM</i>
IC	Rm	0	20K	0
	Rn	NC	47K	NC
	Da	NC	Stuff	NC
NB (Page6)	Ro	NC	20K	20K
	Rp	NC	7.5K	7.5K
	Rq	0	0	0

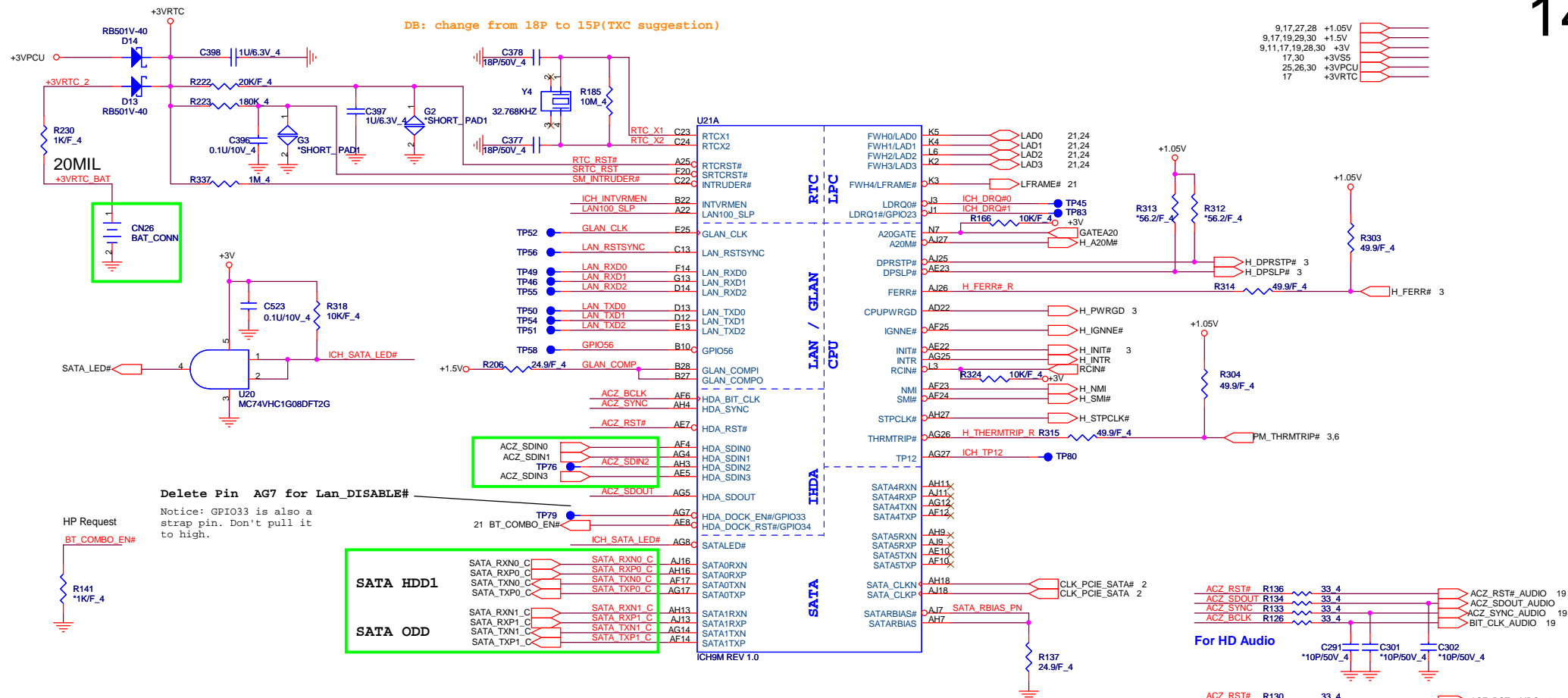


9,11,17,19,28,30 +3V
17,19,30 +5V



PROJECT :AX3
Quanta Computer Inc.

Size Custom	Document Number CRT/HDMI Conn	Rev 2A
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SB Strap

ICH9-M Internal VR
Enable strap
(Internal VR for
VccSus1_05, VccSus1_5
and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for
VccLAN1_05 and
VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

*1K/F_4	R180	GNT0#	15
*1K/F_4	R177	SPI_CS#1_R	

A16 swap override	
strap	Low = A16 swap override enabled
PCI_GNT#3	Hi = Default

*1K/F_4	R178	GNT3#	15
---------	------	-------	----

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

*1K/F_4	R170	ACZ_SPKR	16,19
---------	------	----------	-------

TPM physical presence	
ICH_GPIO57	Low: Default

*10K/F_4	R188	ICH_GPIO57	16
100K/F_4	R189		

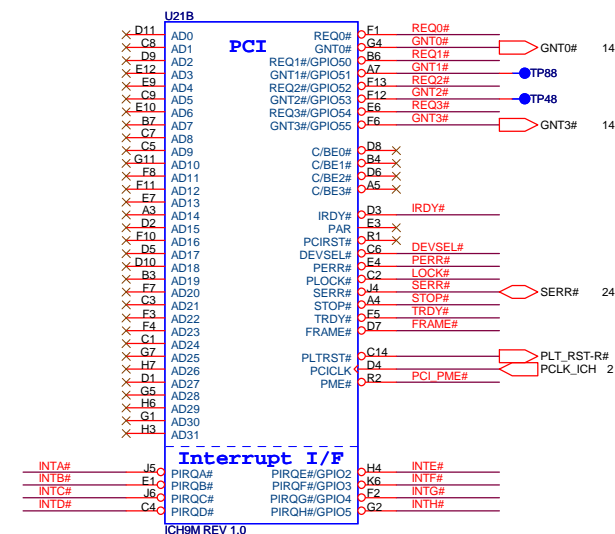
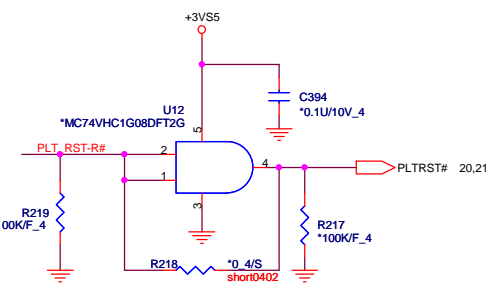
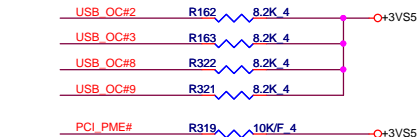
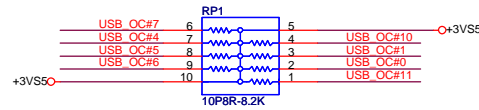
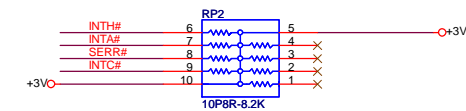
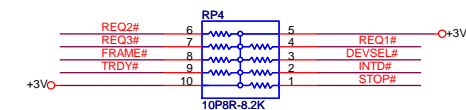
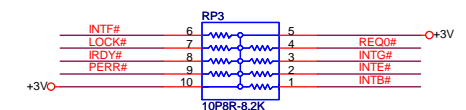
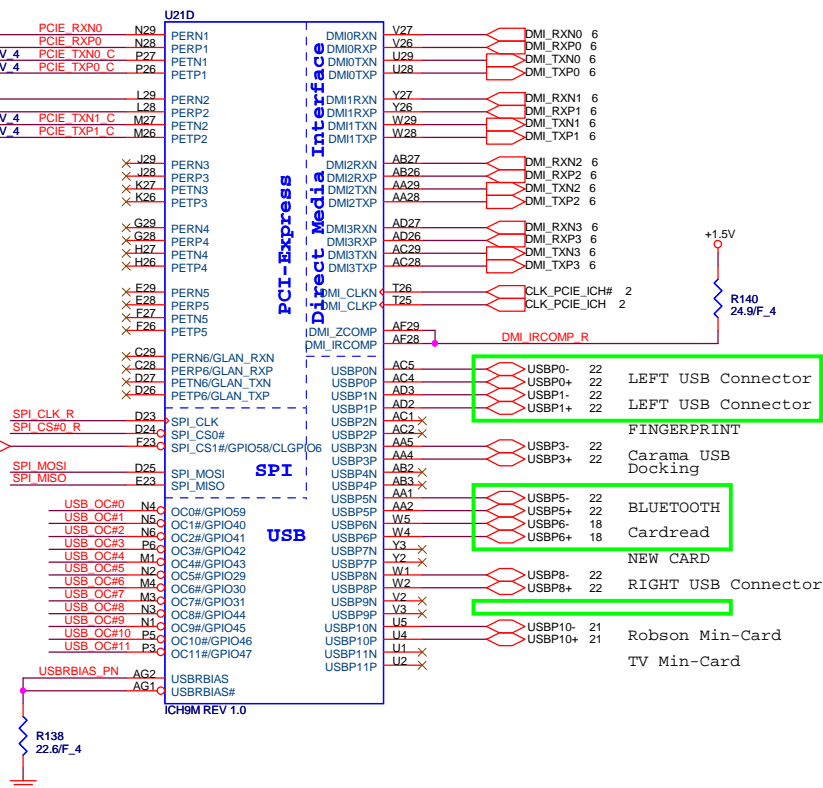
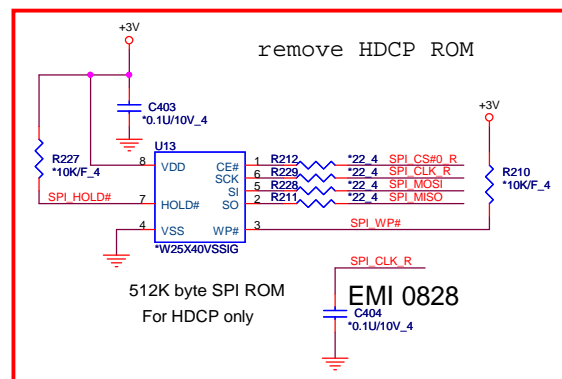


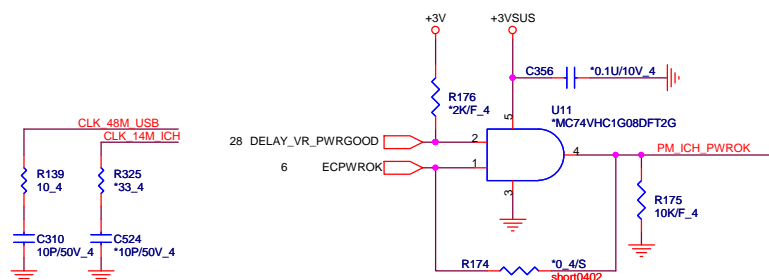
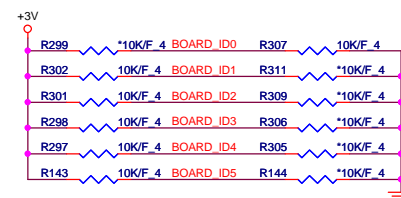
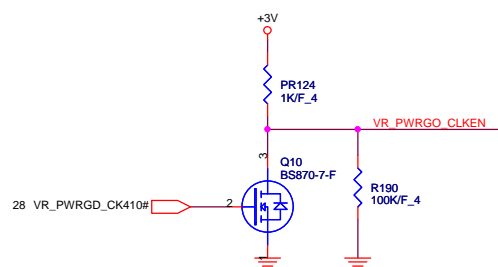
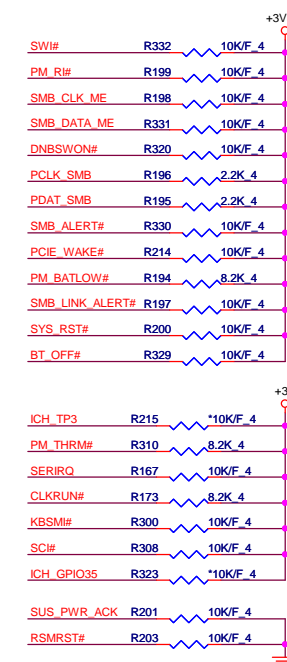
PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M SATA/HDA/RTC 1/4	2A
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MINI CARD PCI-E(WLAN)

PCIE-LAN

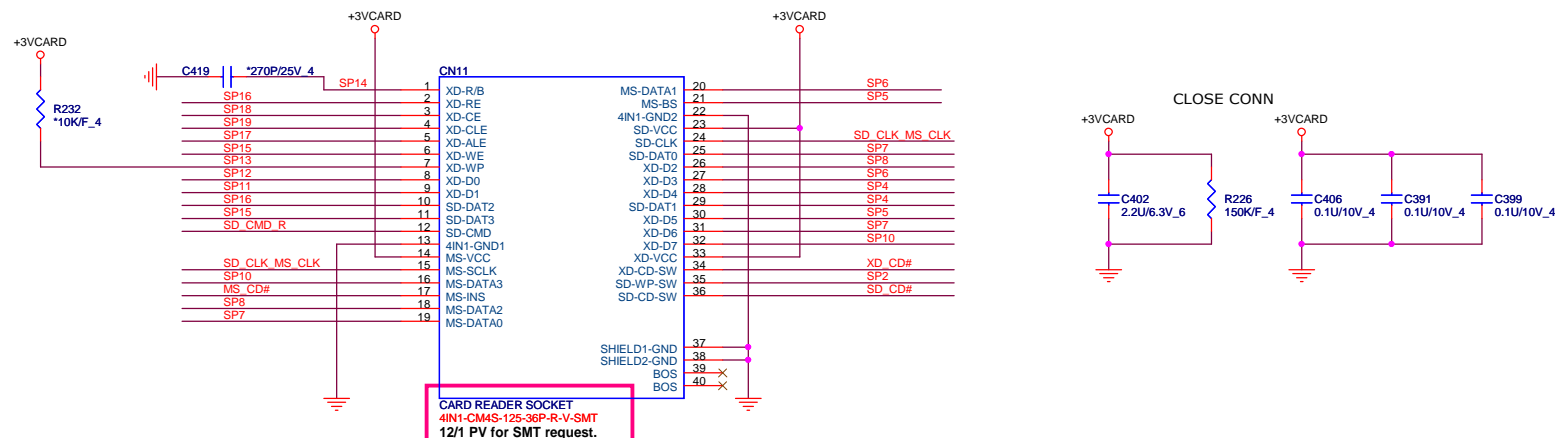
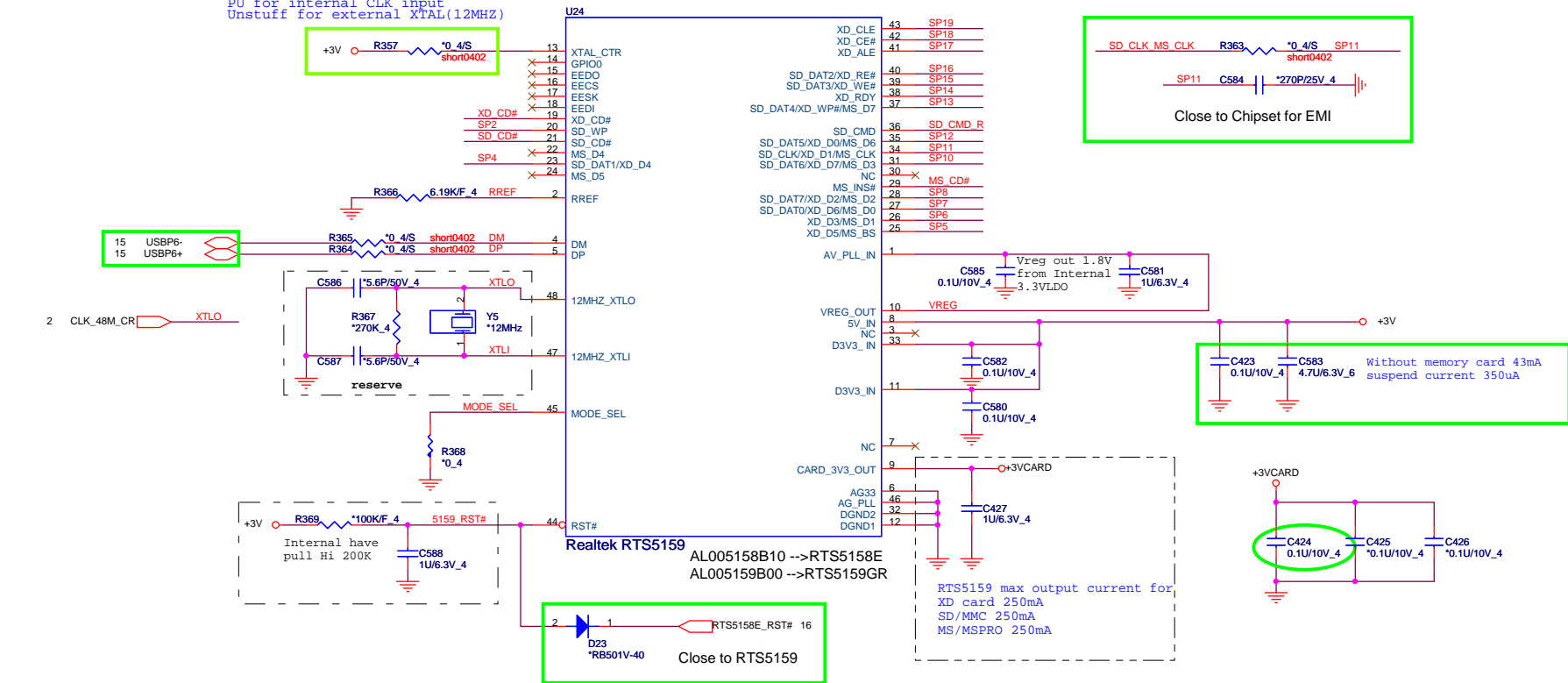




Board ID	ID0 GPIO19	ID1 GPIO21	ID2 GPIO22	ID3 GPIO36	ID4 GPIO37	ID5 GPIO1
UMA/DIS	0=UMA 1=Dis.					
CR/HDMI		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

AX3 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
31AX6MB0000 (CHR)	0	1	1	1	1	1
31AX6MB0010 (PDT)	0	1	1	1	1	1
31AX6MB0020 (PIM)	0	1	1	1	1	1
31AX6MB0030	0	0	1	1	1	1

PU for internal CLK input
Unstuff for external XTAL(12MHZ)



Note:

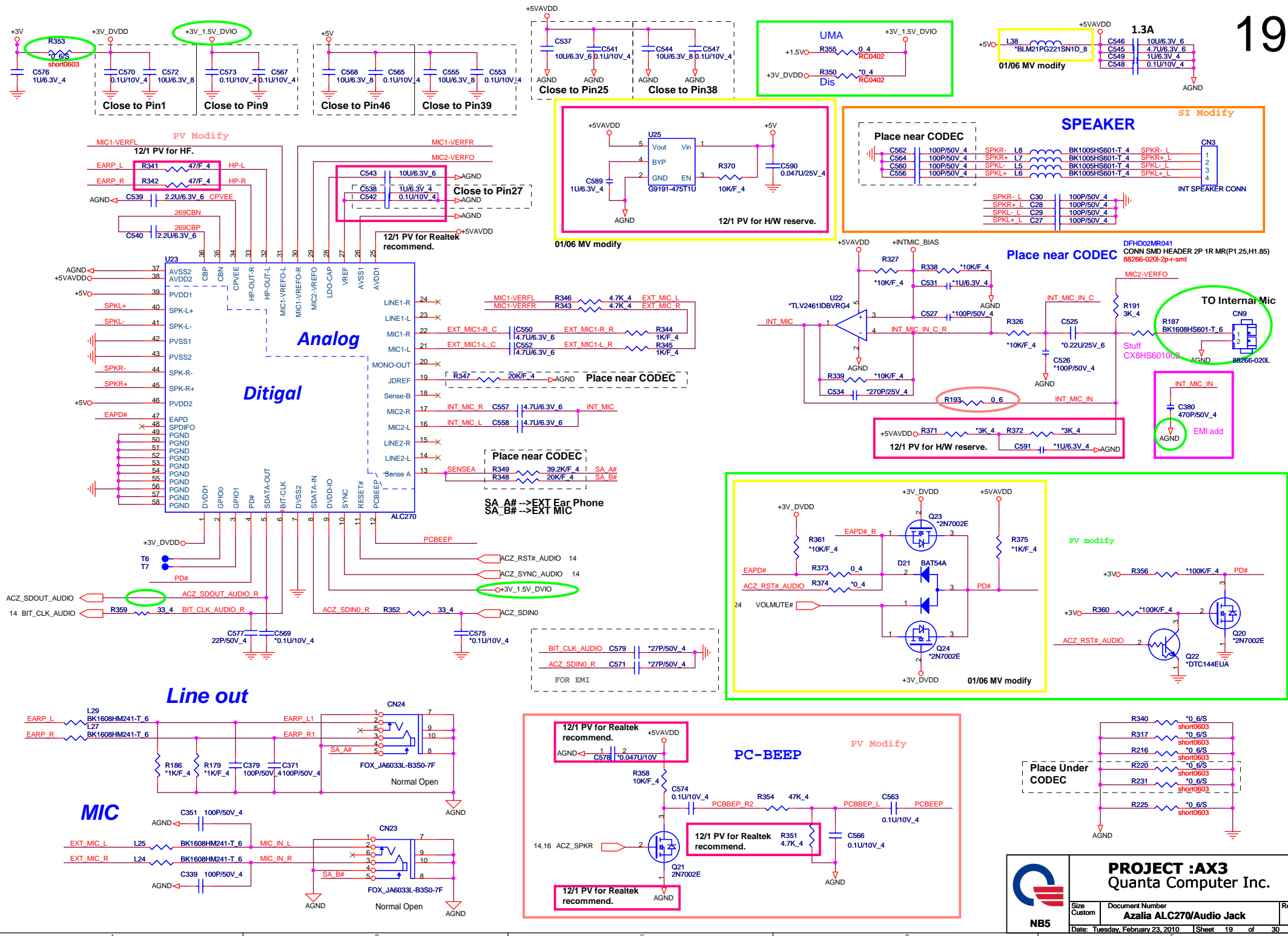
	SD/MMC	MS	XD
SP0			
SP1	SD WP		XD CD#
SP2	SD CD#		
SP3	SD DAT1		XD D4
SP4	SD DAT1		XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4	XD WP#	
SP14		XD R/B#	
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

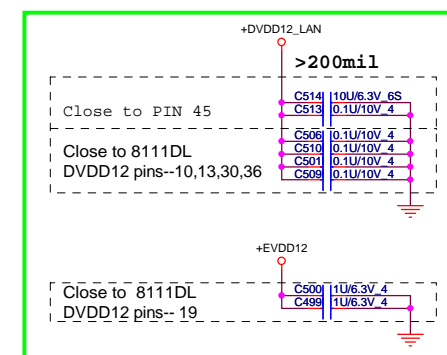


PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159/CR Socket	2A
Date: Tuesday, February 23, 2010 Sheet 18 of 30		

9,11,17,19,28,30 +3V





LAN_EMI

R72

75F_4

LAN_MCT0_2

C218

0.01U/100V_0603

LAN_MX1-

LAN_MX1+

LAN_MCT1

LAN_MX0-

LAN_MX0+

LAN_MCT0

U17

NS681684

RX+

RX-

CT

RX-

TX-

TX+

CMT

TX+

MDI1-

V_DAC_2

C214

0.01U/25V_4

MDI1+

MDI0+

V_DAC_1

C181

0.01U/25V_4

MDI0-

LAN_EMI

R66

75F_4

LAN_MCT0_1

C186

0.01U/100V_0603

C164

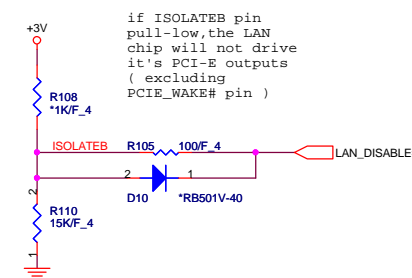
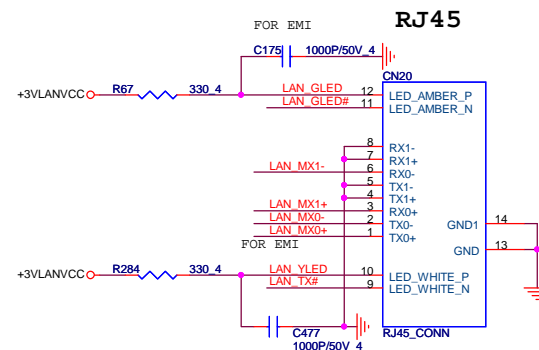
1000P/3KV_1808

CH2100GK112

CC1808

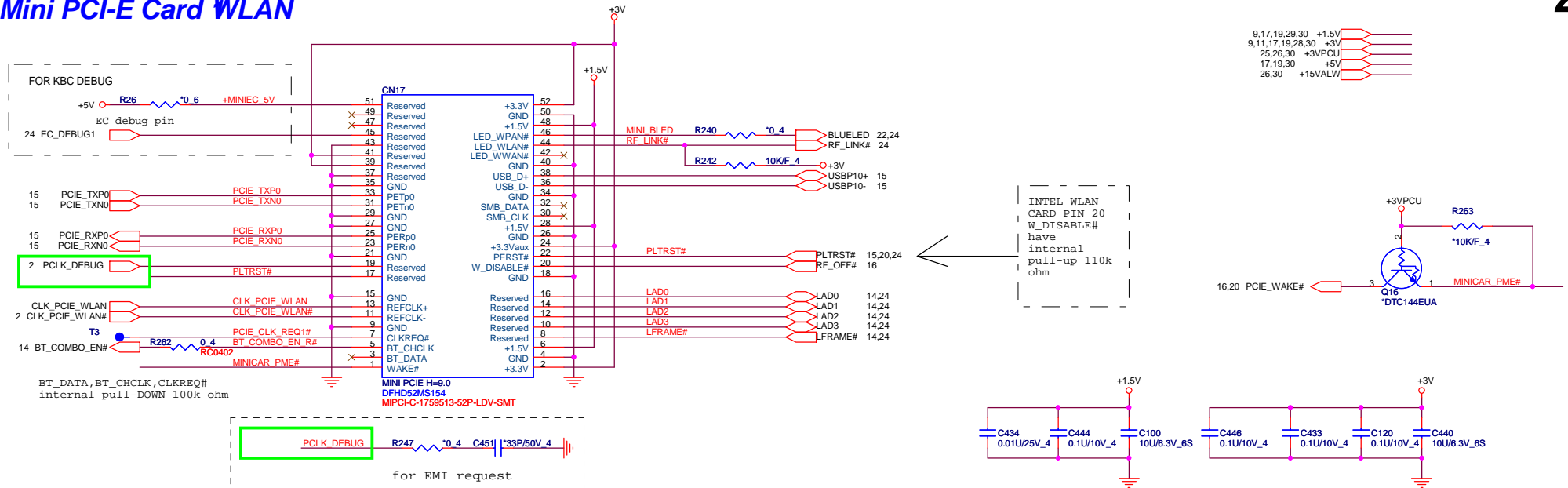
PV modify

The schematic diagram shows the LED driver circuit for the LAN GLINK100#. It features a BAT54A diode connected to the LAN_GLINK100# signal line (pin 1) and the LAN_GLINK10# signal line (pin 2). The diode's cathode is connected to the LAN_GLED# signal line. The anode is connected to the LAN_TX# signal line. A 1/11 MV for EMI filter is connected between the LAN_TX# signal line and ground, consisting of a capacitor C480 (0.01U/25V_4) and a resistor C471 (0.01U/25V_4) in parallel.

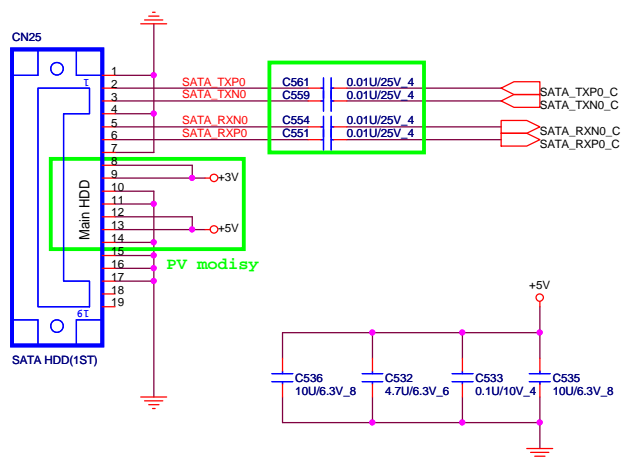


9,11,17,19,28,30 +3V
30 +3VLANVCC

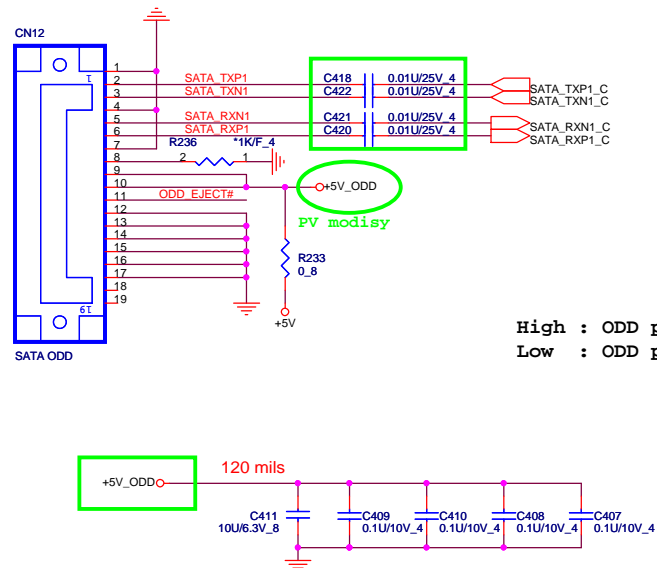
Mini PCI-E Card WLAN



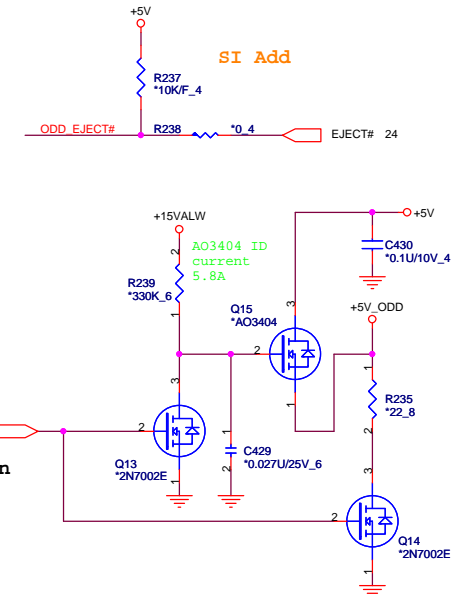
SATA HDD CONNECTOR



SATA ODD CONNECTOR



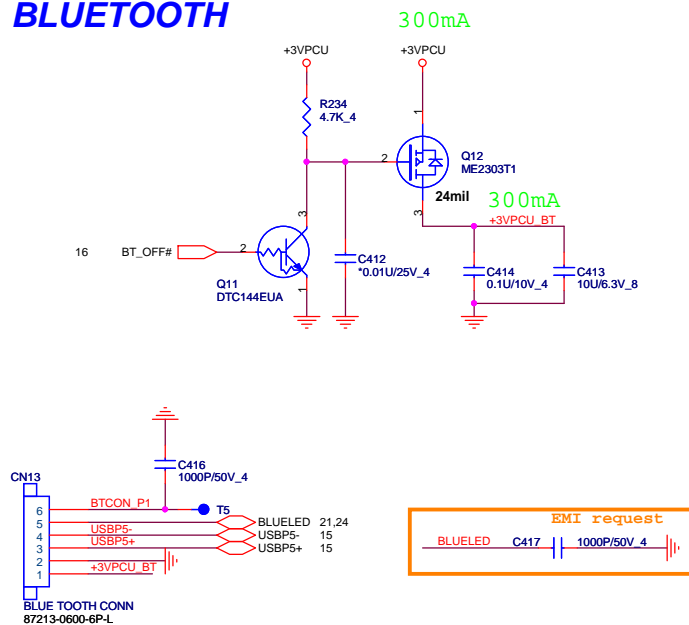
High : ODD power down
Low : ODD power on



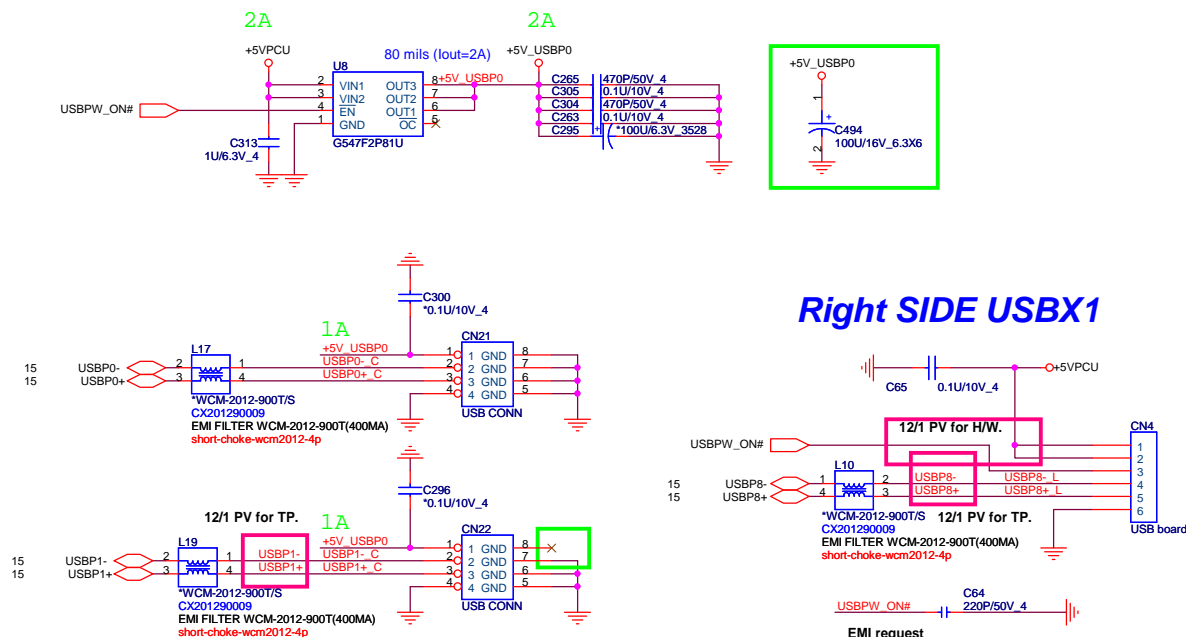
PROJECT :AX3
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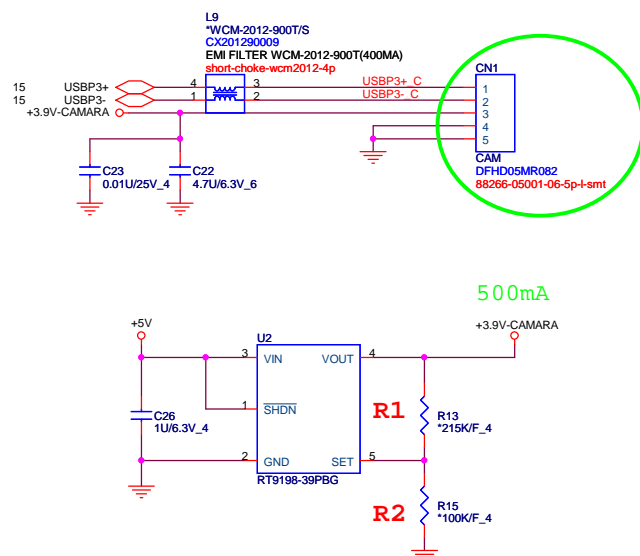
BLUETOOTH



LEFT SIDE USBX1

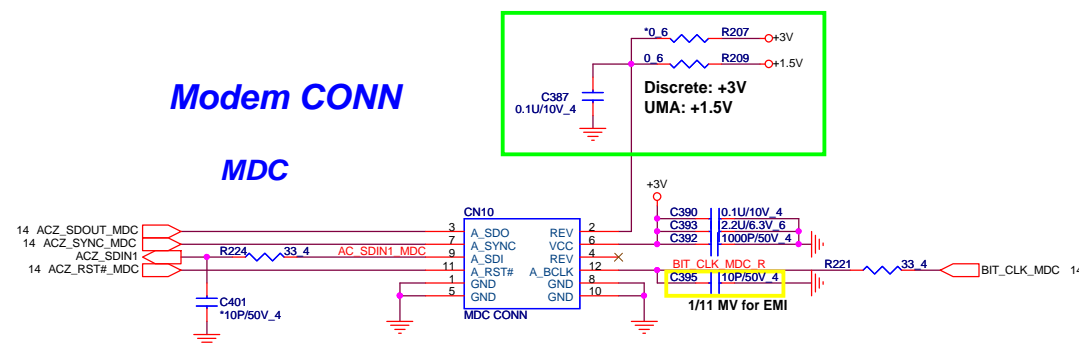



CAMERA



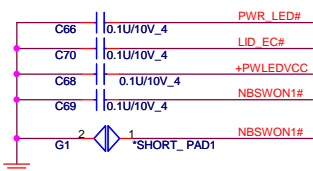
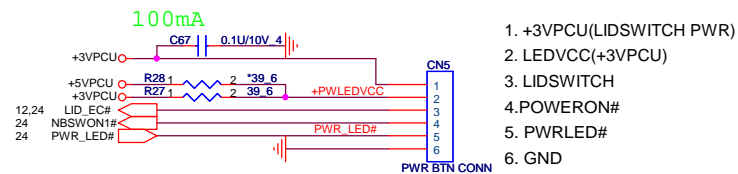
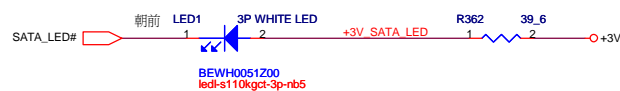
Modem CONN

MDC

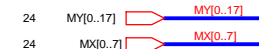
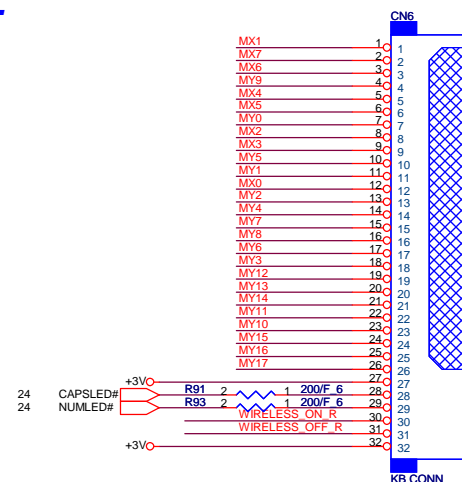
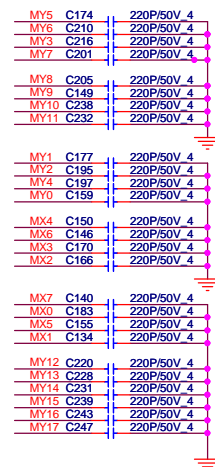




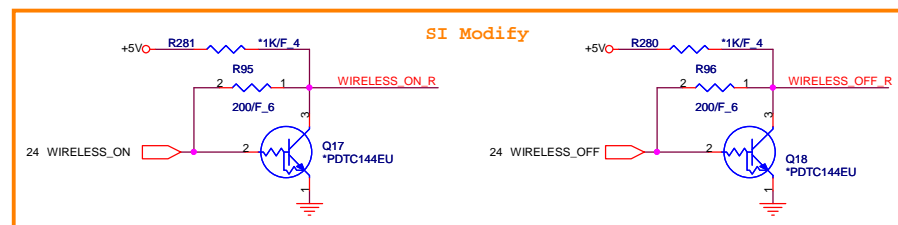
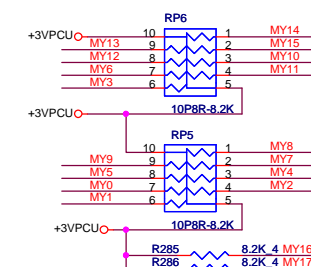
POWER BOTTON CONNECT

**SATA LED**

KEYBOARD Con.

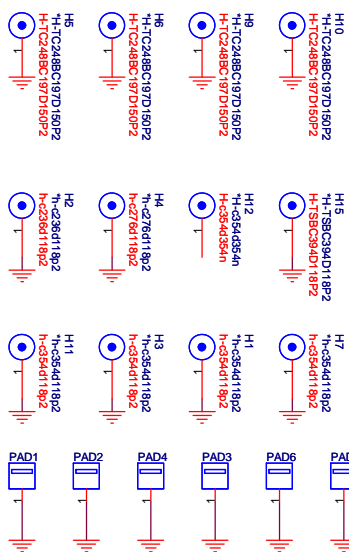


KEYBOARD PULL-UP



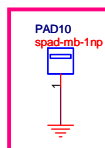
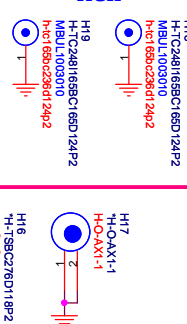
HOLE & PAD

CPU

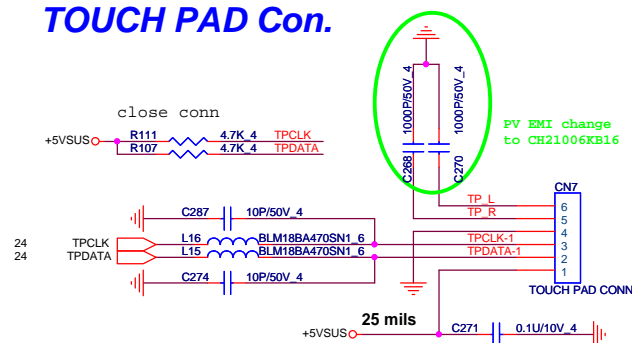


MCH

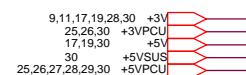
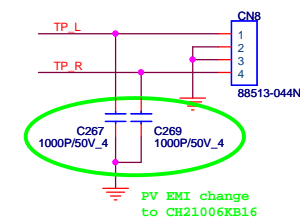
12/10 PV for DXF update.



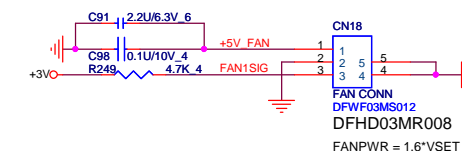
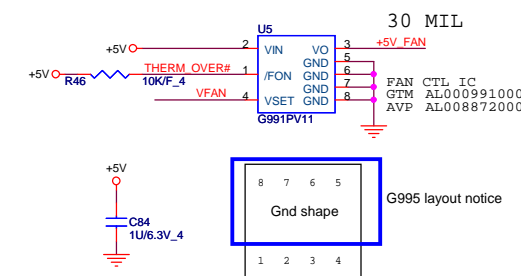
TOUCH PAD Con.



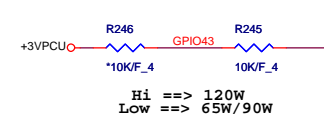
To TOUCH PAD SW board



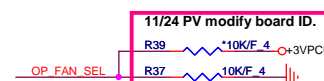
CPU FAN



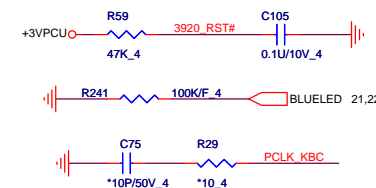
Adapter select for EC



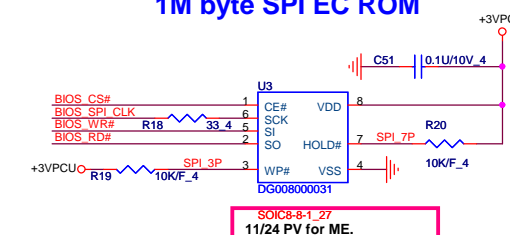
GPIO42 control fan table



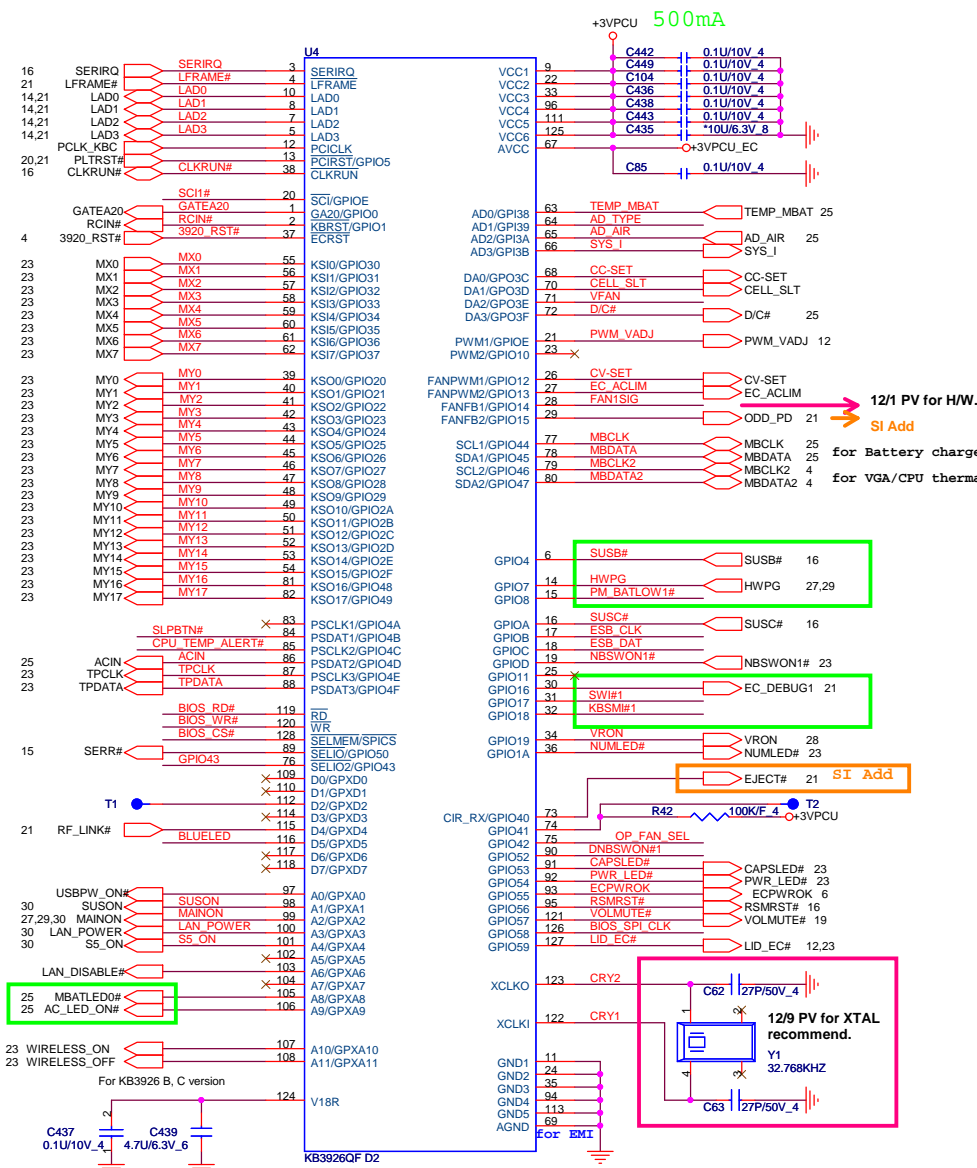
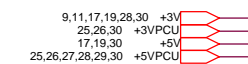
Project Model	GPIO42
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)



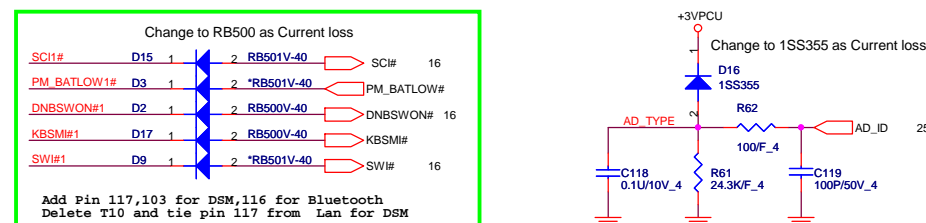
1M byte SPI EC ROM

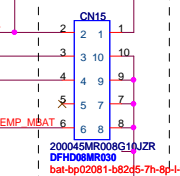


```
Socket: DG008000031
WINBOND AKE3GZN0N00
EON AKE3GZP0Q00
AIT AKE3GZP0801
MAX AKE5GFK0Z09
```



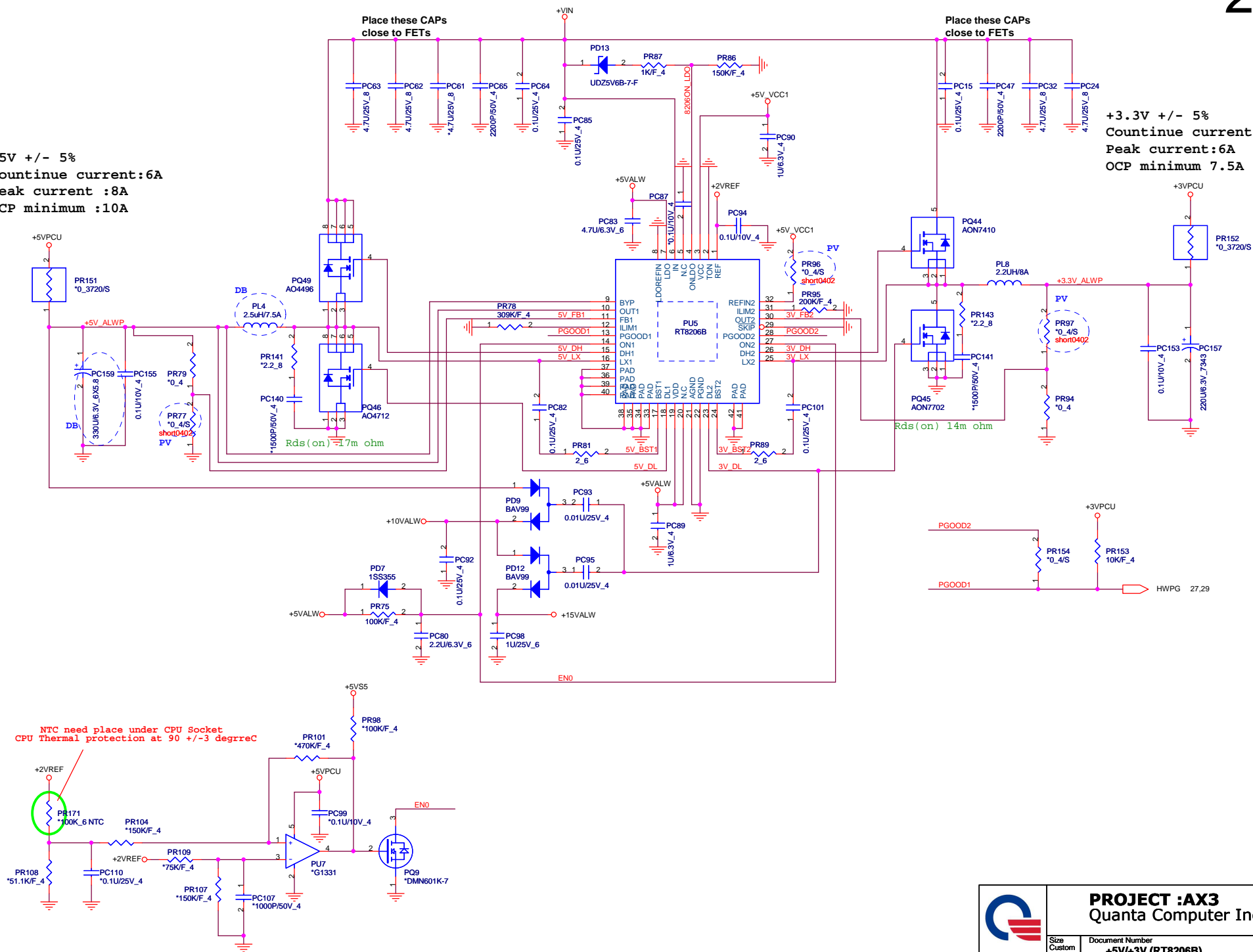
adapter Type check





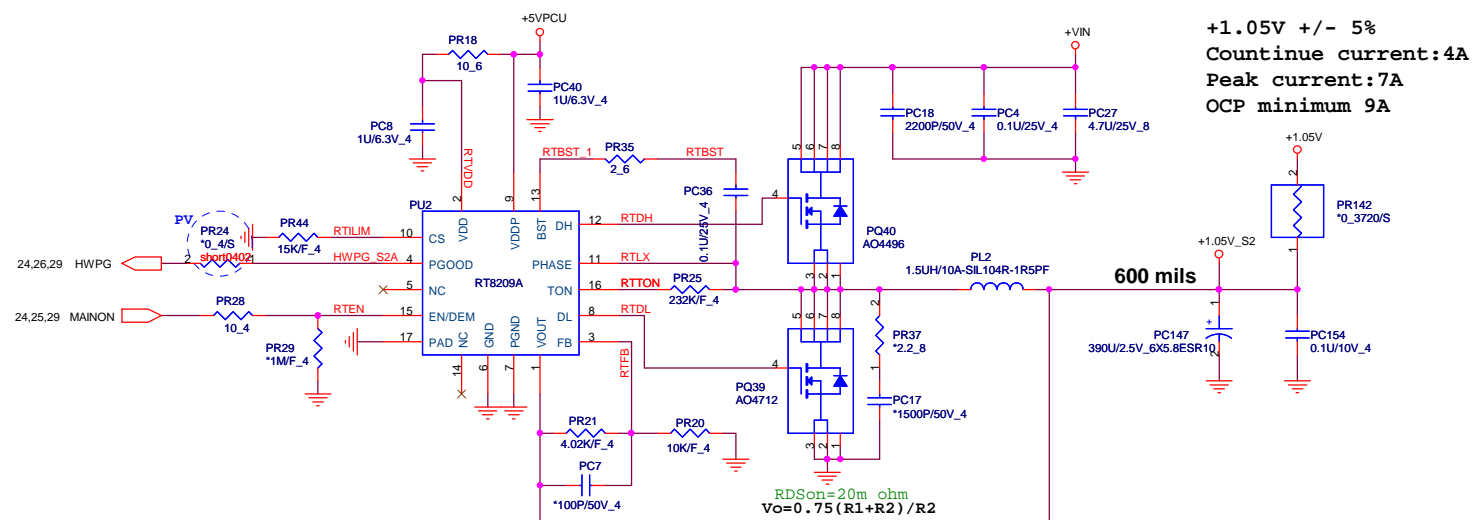
+5V +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A



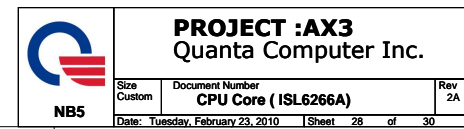
PROJECT :AX3
Quanta Computer Inc.

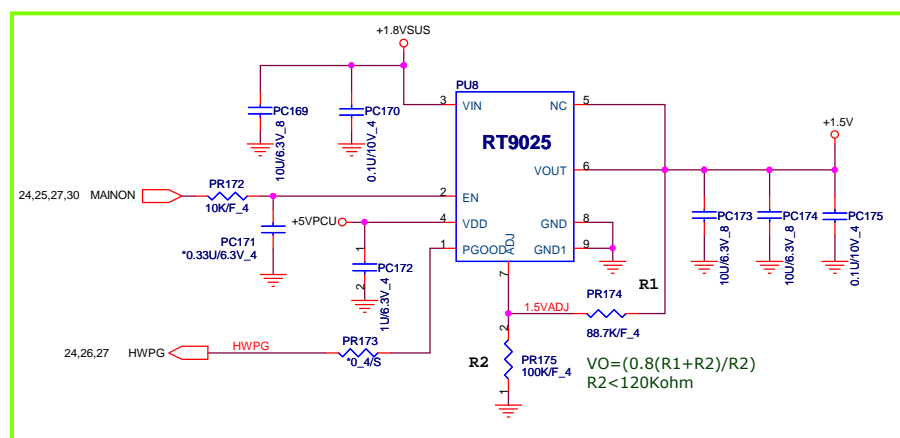
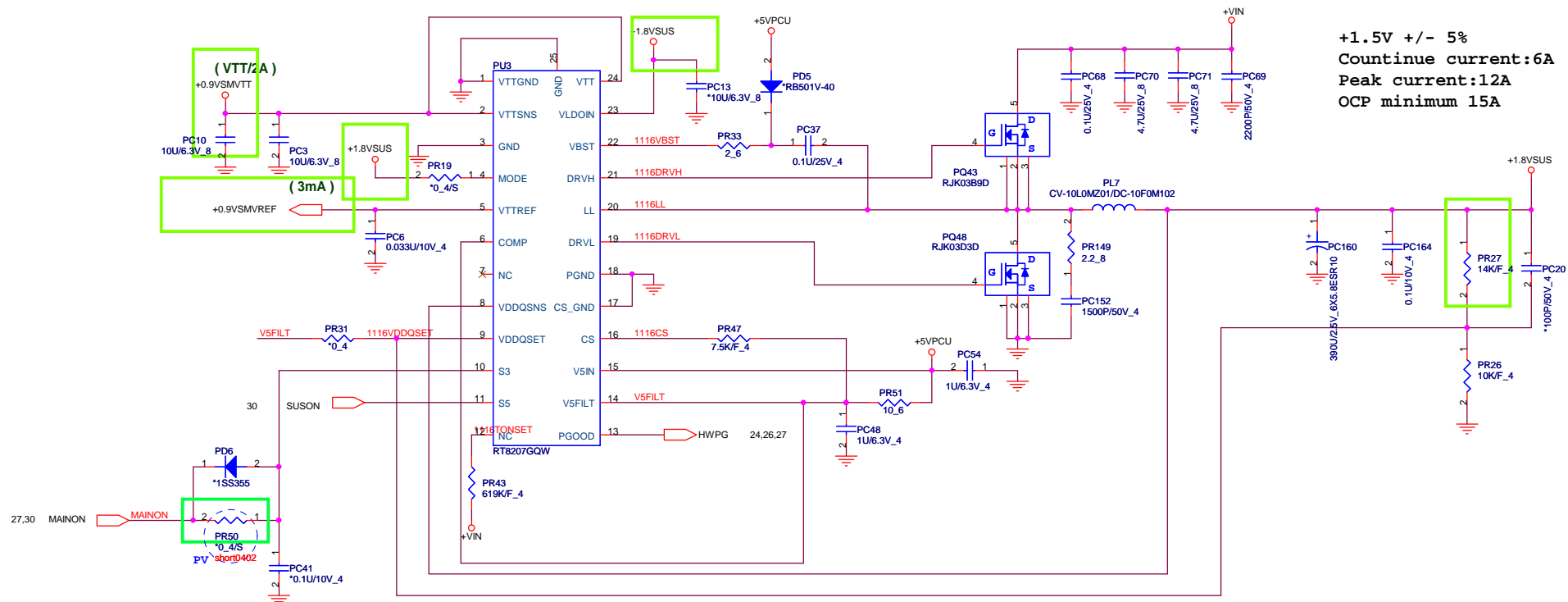
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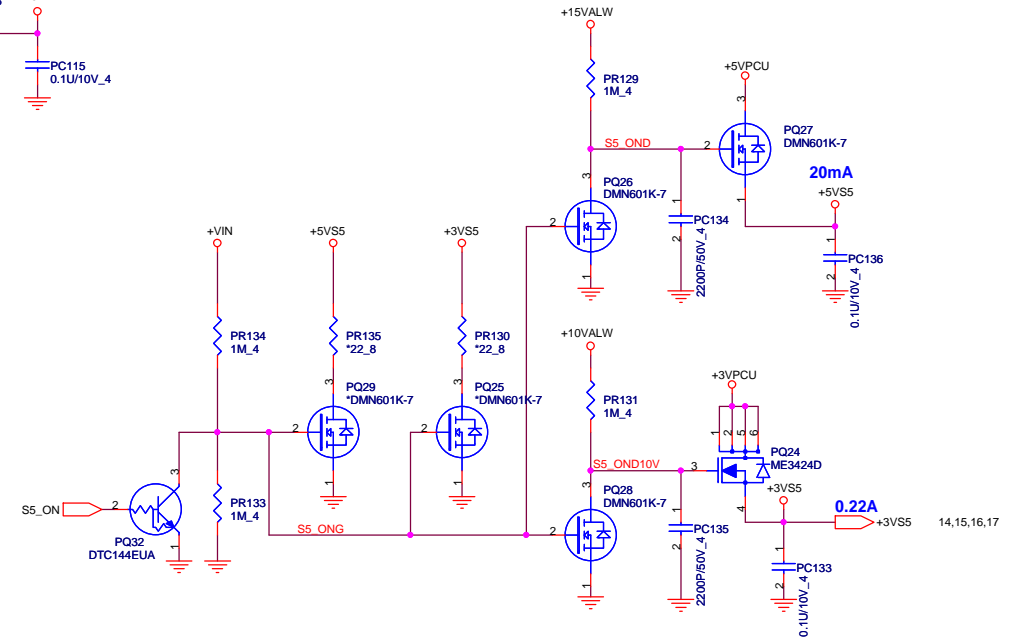
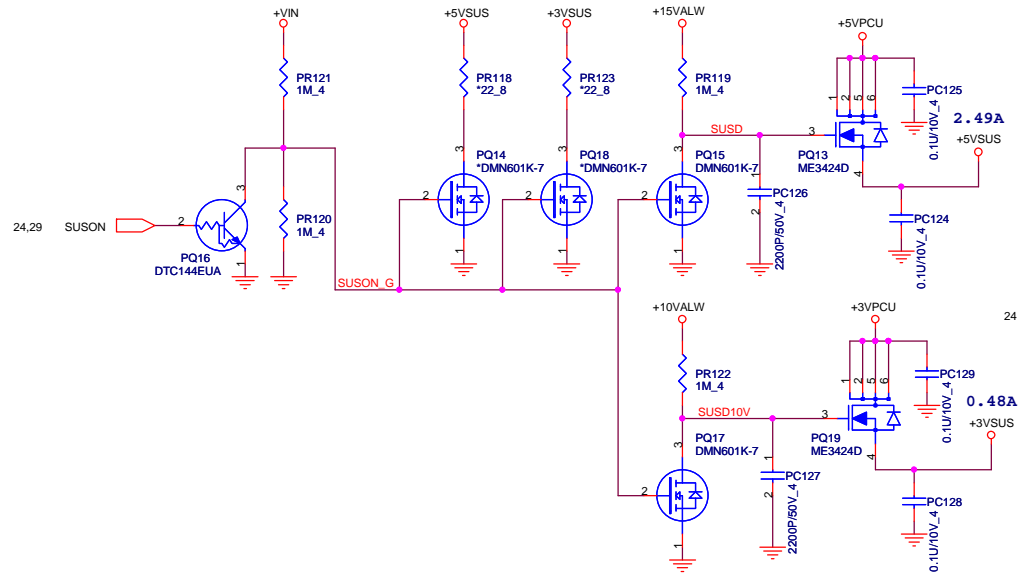
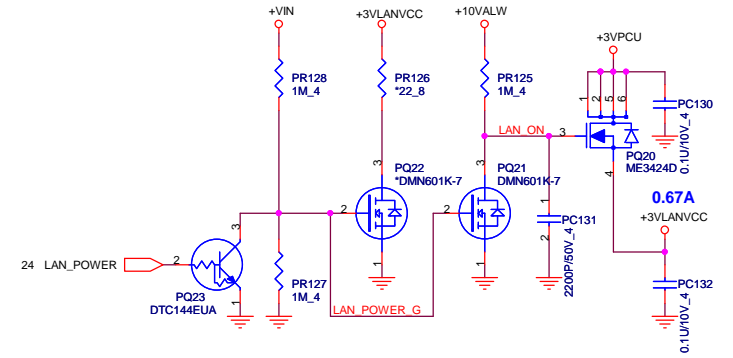
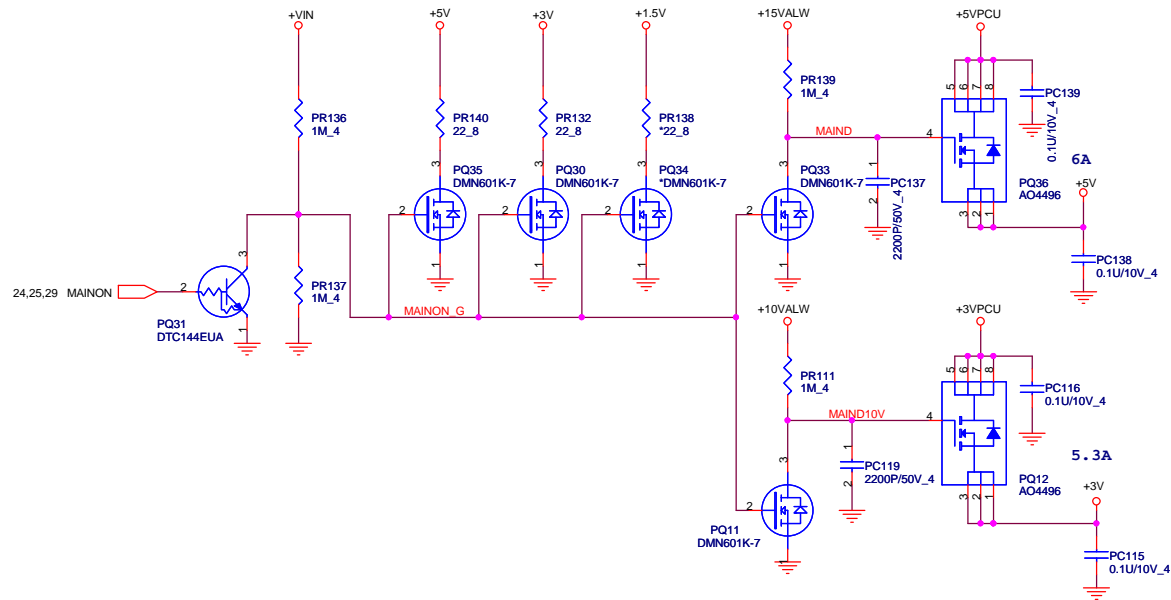


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